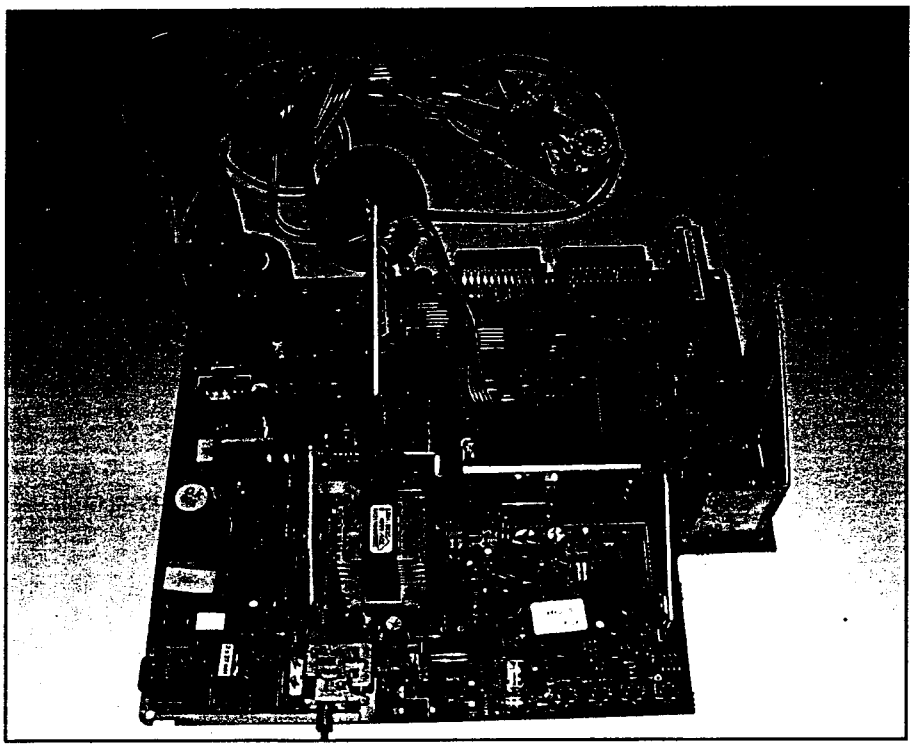
ELEMIS 6570TN CINEMA

MODEL

SERVICE MANUAL

SERVICE MANUAL

PT92 CHASSIS



Modification reserved

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TECHNICAL DATA

CRT PANEL	
Visible Picture	47 cm / 50 cm / 66 cm
Deflection Angle	90°/ 110°
Vertical Frequency	50Hz
Horizontal Frequency	15.625Hz

ELECTRONIC

Program Number	100+AV
Teletext	Flof text
Tuner	Cable tuner - 8 MHz spacing for Hyper Band
TV System	European CCIR system
Music Power	110°2x8 Watt Rms 10% distortion 90°2x4 Watt Rms 10% distortion

CONNECTIONS

Euro AV Socket	Include

MAIN STAGE

Mains Voltage	165-260VAC
Mains Frequency	50Hz
Power Consumption	110° 126W; 90° 75W;
In Stby Mode	110°8 Watt 90°5 Watt

RECOMMENDATION FOR SERVICE REPAIRS

1- Use only original spare parts. Only use components with the same specifications for replacement.
2- Original fuse value only should be used.
3- Main leads and connecting leads should be checked for external damage before connection.
Check the insulation.
4- Parts contributing to the safety of the product must not be damaged or obviously unsuitable.
This is valid especially for insulators and insulating parts.
5- Thermally loaded solder pads are to be sucked off and re-soldered.
6- Ensure that the ventilation slots are not obstructed.
7- Potentials as high as 25 KV are present when this receiver is operating. Operation of the receiver outside the cabinet or with back cover removed involve a shock hazard from the receiver.
Servicing should not be attempted by anyone who is not thoroughly familiar with the precautions necessary when working on high voltage equipment.
Perfectly discharge the high potential of the picture tube before handling the tube. The picture tube is highly evacuated and if broken.
Glass fragments will be violently expelled.
Always discharge the picture tube anode to the receiver chassis to keep of the shock hazard before removing the anode cap.
8- Keep wire away from the high voltage or high temperature components.
9- When replacing a wattage resistor in circuit board, keep the resistor 10 mm away from circuit board.

HANDLING OF MOS CHIP COMPONENTS

MOS circuit requires special attention with regard to static charges. Static charges may occur with any highly insulating plastics and can be transferred to persons wearing clothes and shoes made of synthetic materials. Protective circuits on the inputs and outputs of mos circuits give protection to a limited extend only due to time of reaction.

Please observe the following instructions to protect the components against damage from static charges.

1- Keep mos components in conductive package until they are used. Most components must never be stored in styropor materials or plastic magazines.
2- Persons have to rid themselves of electrostatic charges by touching MOS components.
3- Hold the component by the body touching the terminals.
4- Use only grounded instruments for testing and processing purposes.
5- Remove or connect MOS ICs when operating voltage is disconnected.

X-RAY RADIATION PRECAUTION

1- Excessive high voltage can be produce potentially hazardous X-RAY radiation. To avoid such hazard, the high voltage must not be above the specified limit. The nominal value of the high voltage of this receiver is 25KV at zero beam current (minimum brightness) under 220V AC power source. The high voltage must not under any circumstance, exceed 30KV. It is recommended the reading of the high voltage be recorded as a part of the service record. It is important to use an accurate and reliable high voltage meter.
2- The primary source of X-RAY radiation in this TV receiver is the picture tube. For continued X-RAY radiation protection, the replacement tube must be exactly the same type tube as specified in the part list.

SERVICE MENU

The service menu is entered by pressing the <SUB-PAGE> key on the RC and VOLUME-DOWN key on the TV simultaneously when the TV is in TV- mode. The service menu is left by pressing the <TV> key.

When entering the service mode the first menu item is IF (selection of normal IF). Next items can be selected using the keys <PROGRAM-UP> and <PROGRAM-DOWN>. The value of each item can be changed using the keys <VOLUME-UP> and <VOLUME-DOWN>. The item values are displayed as decimal values, except for the tuner-band-selection, BITS and option items.

They are displayed as hexa-decimal values. All values are stored in non-volatile memory when the service menu is left. The "INIT CTV832U" item initializes the NVM: It clears all names and tuning information of all programs and writes default values for the service alignments and preset values in NVM. While doing so, the OSD displays "BUSY". When the initialization is finished, the message "READY" is written on the screen.

Item	Default	Explanation
IF	38.9	IF selection (58.8, 45.8, 38.9 or 38.00 MHz)
IFL1	33.9	IF for SECAM-L1 selection (33.4 or 33.9 MHz)
HP	31	Horizontal parallelogram
HB	31	Horizontal bow
EW	37	East-west Width for picture setting 16:9
PW	18	East-west Parabola for picture setting 16:9
UCP	13	East-west Upper Corner parabola for picture setting 16:9
LCP	13	East-west Lower Corner parabola for picture setting 16:9
TC	28	East-west Trapezium for picture setting 16:9
HP4:3	31	Horizontal parallelogram for picture setting 4:3
HB4:3	31	Horizontal bow for picture setting 4:3
EW4:3	45	East-west Width for picture setting 4:3
PW4:3	15	East-west Parabola for picture setting 4:3
UCP4:3	35	East-west Upper Corner parabola for picture setting 4:3
LCP4:3	25	East-west Lower Corner parabola for picture setting 4:3
TC4:3	31	East-west Trapezium for picture setting 4:3
HS	31	Horizontal Shift
VS	31	Vertical Slope
VA	31	Vertical Amplitude
SC	31	S-Correction
VSD	off	Vertical Scan Disable
VSH	31	Vertical Shift
VX	25	Vertical zoom (East-west only)
BLR	7	Black Level Red
BLG	7	Black Level Green
WPR	31	White point correction Red
WPG	31	White point correction Green
WPB	31	White point correction Blue
Ys	15	Y-delay adjustment for SECAM
Yn	8	Y-delay adjustment for NTSC
YP	0	Y-delay adjustment for PAL

Yo	0	Y-delay adjustment for external sources
AGC	4	AGC take over
CL	4	Cathode drive level
Bits	00	(ACL=0; FCO= 0; SVO= 0; HP2= 0; FSL= 0; OSO= 0)
Bits1	00	(FFI= 0; TV= 0; AV-1= 0; AV-2= 0; AV-2S= 0; AV-3= 0; AV-3S= 0; AV = 0)

OptByte1 **(Default=E3)**

PAL-BG	=	Selection PAL-BG	(1)
PAL-DK	=	Selection PAL-DK	(1)
PAL-I	=	Selection PAL-I	(0)
PAL-M	=	Selection PAL-M	(0)
PAL-N	=	Selection PAL-N	(0)
NTSC-M	=	Selection NTSC-M	(1)
NTSC-443	=	Selection NTSC-443	(1)
SECAM-BG	=	Selection SECAM-BG	(1)

*(1) Selected, (0) Not Selected

OptByte2 **(Default=07)**

SECAM-DK	=	Selection SECAM-DK	(1)
FRANCE	=	Selection FRANCE	(1)
Logo	=	Enable/Disable Logo	(1/0)
PalBG Scr	=	When the PalBG Scr selected, TV searches only PalBG. Otherwise it searches all.	(0)
AV2	=	Selection AV2	(0)

*(1) Selected, (0) Not Selected

OptByte3 **(Default=E8)**

HP	=	Selection HP	(0)
Volbar	=	Selection Volbar	(1)
Subwof	=	Selection Subwof	(0)
Presets	=	Selection Presets	(1)
Lock	=	Selection Lock	(1)
Hotel	=	When the Hotel mode selected, It's impossible to enter menu settings.It selects the Hotel mode.	(1)

*(1) Selected, (0) Not Selected

OptByte4 **(Default=B8)**

16:9	=	Set 16:9 mode active	(1)
110	=	Selection 110/90 Tube	(1/0)
Hpol	=	Default	(0)
Vpol	=	Default	(0)
Field	=	Default	(1)
FE-Out	=	Default	(1)
Sw-on	=	When the power on the TV, it Enables or Disables Standby Mode.	(1/0)
Vg-Check	=	Default	(1)

*(1) Selected, (0) Not Selected

OptByte5 **(Default=09)**

Clock	=	Enable/Disable Clock Menu	(1)
AM/PM	=	Default	(0)
AVL	=	Auto Volume Level	(1)
1-norma	=	Default	(0)

*(1) Selected, (0) Not Selected

OptByte6 **(Default=00)**

UOC-J	=	Default	(0)
ignrSUP	=	Default	(0)
ignrNDF	=	Default	(0)

*(1) Selected, (0) Not Selected

TSL	45	Start frequency of the low-band in MHz
TEL	118	End frequency of the low-band
TSM	118	Start frequency of the mid-band
TEM	400	End frequency of the mid-band
TSH	400	Start frequency of the high-band
TEH	863	End frequency of the high-band
TBL	03	hex Value needed for switching to the low-band
TBN	06	hex Value needed for switching to the mid-band
TBH	85	hex Value needed for switching to the high-band

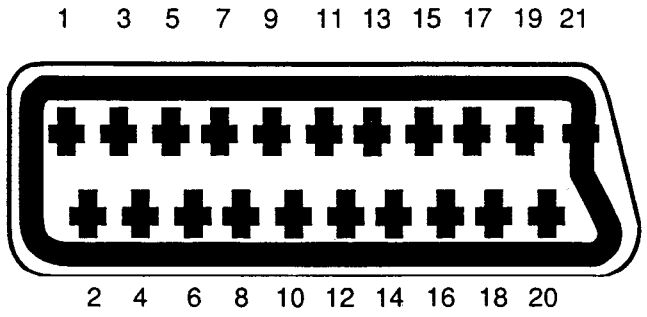
16:9 / 4:3 Adjustment

The CTV832U software uses two sets of parameters for the registers HP (horizontal parallelogram), HB (horizontal bow), EW (EW width), PW (parabola/width), UCP (upper corner parabola), LCP (lower corner parabola) and IC (EW trapezium). They occur in the service menu for 16:9 screen with the listed abbreviations.
For the 4:3 screen there is a second set of these registers. They occur in the service menu with the extension '4:3' (i.e. HP4:3, HB4:3,...).
Each register set must be adjusted under the right conditions i.e. the 16:9 settings are adjusted with a 16:9 picture - the 4:3 settings with a 4:3 picture.
The inenu items EW, PW, UCP, LCP, TC, HP4:3, HB4:3,... TC4:3 and VX will only be in the service menu if the option 16:9 is set in 4 th option byte.

TUNER PARAMETER IN SERVICE AND DEFINITION		PHILIPS	OREGA	TEMIC	SAMSUNG	ALPS
TSL	Start frequency of the low-band in MHz	45	45	45	45	45
TEL	End frequency of the low-band	160	118	150	150	180
TSM	Start frequency of the mid-band	160	118	150	150	180
TEM	End frequency of the mid-band	440	400	440	425	465
TSH	Start frequency of the high-band	440	400	440	425	465
TEH	End frequency of the high-band	863	865	865	865	900
TBL	hex Value needed for switching to the low-band	A1	03	01	01	01
TBN	hex Value needed for switching to the mid-band	92	06	02	02	02
TBH	hex Value needed for switching to the high-band	34	85	04	08	0C

SPECIFICATION OF THE CONNECTOR (EURO SCART)

I- Audio output 1. right channel 0.5 VRMS/<l k 0
2- Audio input 1. right channel 0.5 VRMS (connected to No.6)
3- Audio output 2. left channel 0.5 VRMS (connected to No.1)
4- GND (audio)
5- GND
6- Audio input 2. left channel 0.5 VRMS/>10k 0
7- RGB input, blue (B)
8- Switch signal video (status)
9- GND
10- Reserved for clock signals (not connected)
11- RGB input, green (G)
12- Reserved for remote control (not connected)
13- GND
14- GND switch signal RGB
15- RGB input, red (R)
16- Switch signal RGB
17- GND (video)
18- GND19- Video output 1 Vpp/75 ohm
20- Video input 1 Vpp/75 ohm
21- Shield



TV-Chassis PT-92 / 32"

stereo, 2 Scart, DVD-Player CTV 482 ST/VT

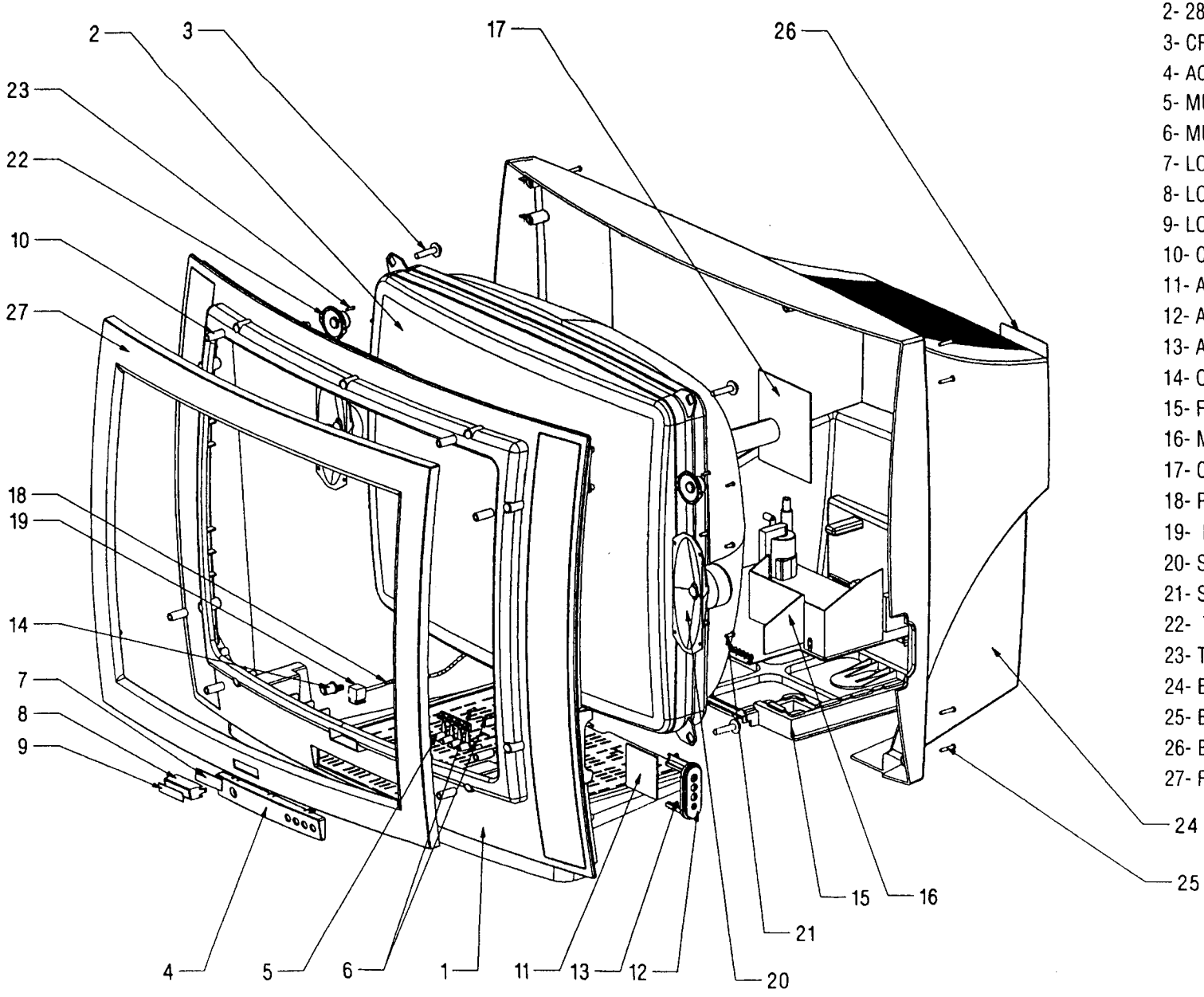
TDA 9353PS/N1/3L0306
TDA 9353D1

IF	38,9
IFL1	33,4od.,9
HP	34
HB	35
EW	45
PW	12
UCP	1
LCP	13
TC	32
HP4:3	22
HB4:3	31
EW4:3	29
PW4:3	15
UCP4:3	1
LCP4:3	13
TC4:3	28
HS	29
VS	28
VA	44
SC	5
VSH	29
VX	25
BLR	8
BLG	10
WPR	49
WPG	36
WPB	32
Ys	5
Yn	5
Yp	5
Yo	5
AGC	20
CL	8
obige Werte können je nach Bildröhrentyp variieren	

Bits0	00	Opt3	6C
ACL	0		0
FCO	0	Jr	0
SVO	0	HP	1
HP2	0	Volbar	1
FSL	0	SubWoof	0
OSO	0	Presets	1
	0	Lock	1
	0	Hotel	0
Bits1	00	Opt4	B3
FFI	0	16:9	1
BTSC	0	110	1
FMWS	0	Hpol	0
BKS	0	Vpol	0
	0	Field	1
	0	Fe-Out	1
	0	Sw-on	0
	0	VG-Check	1
Opt1	01	Opt5	05
PAL-BG	1	Clock	1
PAL-DK	0	AM/PM	0
PAL-I	0	AVL	0
PAL-M	0		0
PAL-N	0	1-norma	0
NTSC-M	0		0
NTSC-443	0		0
SECAM-BG	0		0
Opt2	1C	Opt6	40
SECAM-DK	0	UOC-J	0
FRANCE	0	ignrSUP	0
DVD	1	ignrNDF	0
PalBg Src	1	PAL-BG/DK	0
AV2	1	PAL-L	0
	0	Eco	0
	0	DVD Start	1
	0	WSS	0

Tunerwerte

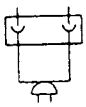
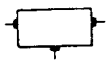
TSL	045
TEL	118
TSM	118
TEM	400
TSH	400
TEH	863
TBL	03
TBM	06
TBH	85

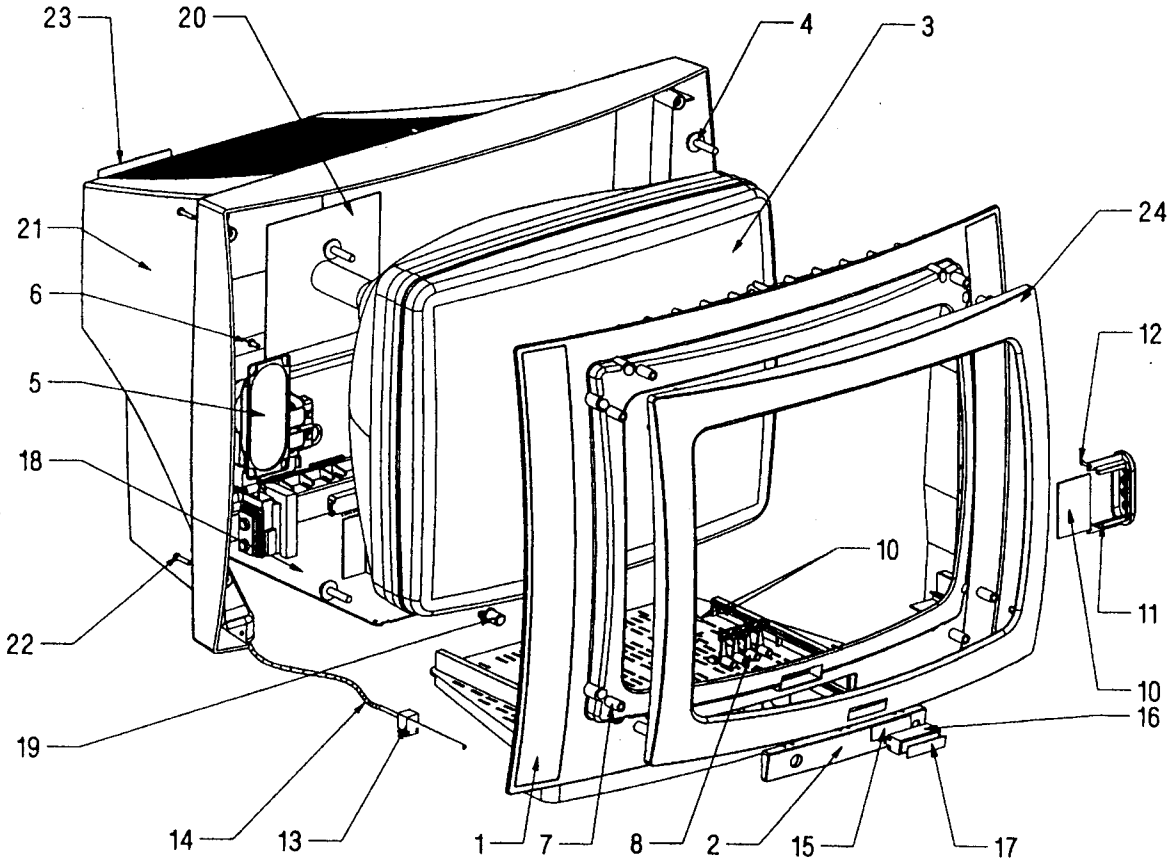


1- 28" MEGA CABINET
2- 28" FST CRT
3- CRT SCREW Ø 7x30
4- ACRYLIC WINDOW
5- MULTIPLE BUTTON
6- MULTIPLE BUTTON SCREW Ø 2.9x9.5
7- LOGO PCB
8- LOGO ACR.
9- LOGO
10- CRT PANEL STOPER
11- AV PCB
12- AV PCB HOLDER
13- AV HOLDER SCREW
14- ON-OFF BUTTON
15- FRAME MAIN PCB
16- MAIN PCB
17- CRT PCB
18- POWER CABLE
19- POWER CABLE HOLDER
20- SPEAKER
21- SPEAKER SCREW
22- TWEETER
23- TWEETER SCREW
24- BACK COWER
25- BACK COWER SCREW
26- BACK COWER LABEL
27- FRONT FRAME

28" MEGA CTV

COMPONENT DESCRIPTIONS

	POWER CORD
	SAW FILTER
	IR SENSOR
	VOLTAGE REGULATOR
	ON/OFF SWITCH
	LINE FILTER
	PTC
	NPN TRANSISTOR
	PNP TRANSISTOR
	CERAMIC FILTER
	COIL
	LINEARITY COIL
	FUSIBLE RESISTOR
	IW METAL OXIDE RESISTOR
	1/2W METAL OXIDE RESISTOR
	1/4 OR 1/6W CARBON FILM RESISTOR
	CERAMIC CAPACITOR /POLYESTER CAPACITOR
	ELECTROLYTIC CAPACITOR
	DIODE
	ZENER DIODE
	SWITCH JUMPER
	NET (INPUT)
	NET (OUTPUT)
	TACT SWITCH

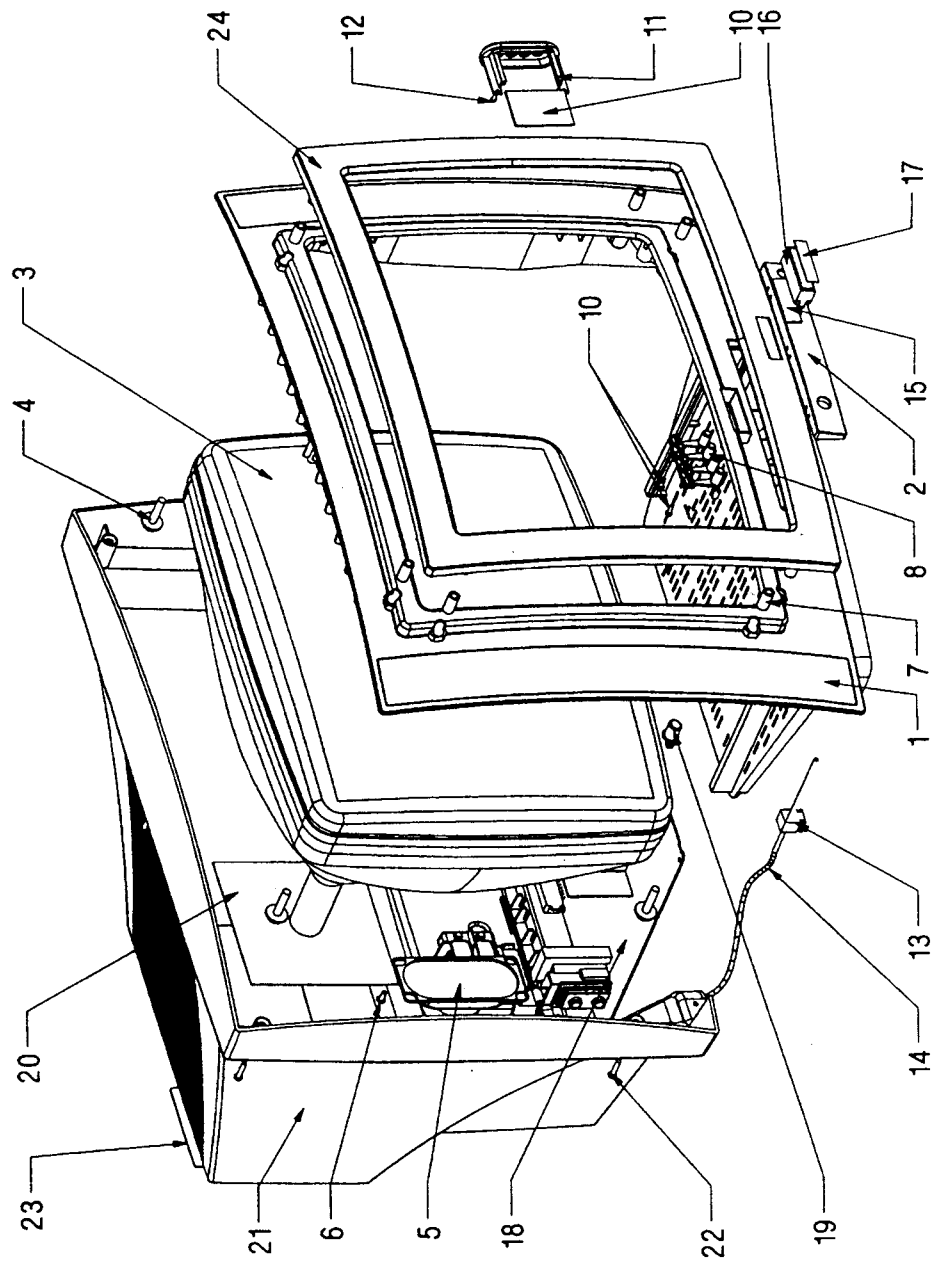


1- 20" MEGA CABINET
2- ACRYLIC WINDOW 20" CRT
3- 20" CRT
4- CRT SCREW Ø 7x30
5- SPEAKER
6- SPEAKER SCREW Ø 3.9x10
7- CRT RUBBER
8- MULTIPLE BUTTON
9- MULTIPLE BUTTON SCREW Ø 2.9x9.5
10- AV PCB
11- AV PCB HOLDER
12- AV HOLDER SCREW Ø 2.9x9.5
13- POWER CABLE HOLDER
14- POWER CABLE
15- LOGO PCB
16- LOGO ACR.
17- LOGO
18- MAIN PCB
19- ON-OFF BUTTON
20- CRT PCB
21- BACK COWER
22- BACK COWER SCREW Ø 3.9x19
23- BACK COWER LABEL
24- FRONT FRAME

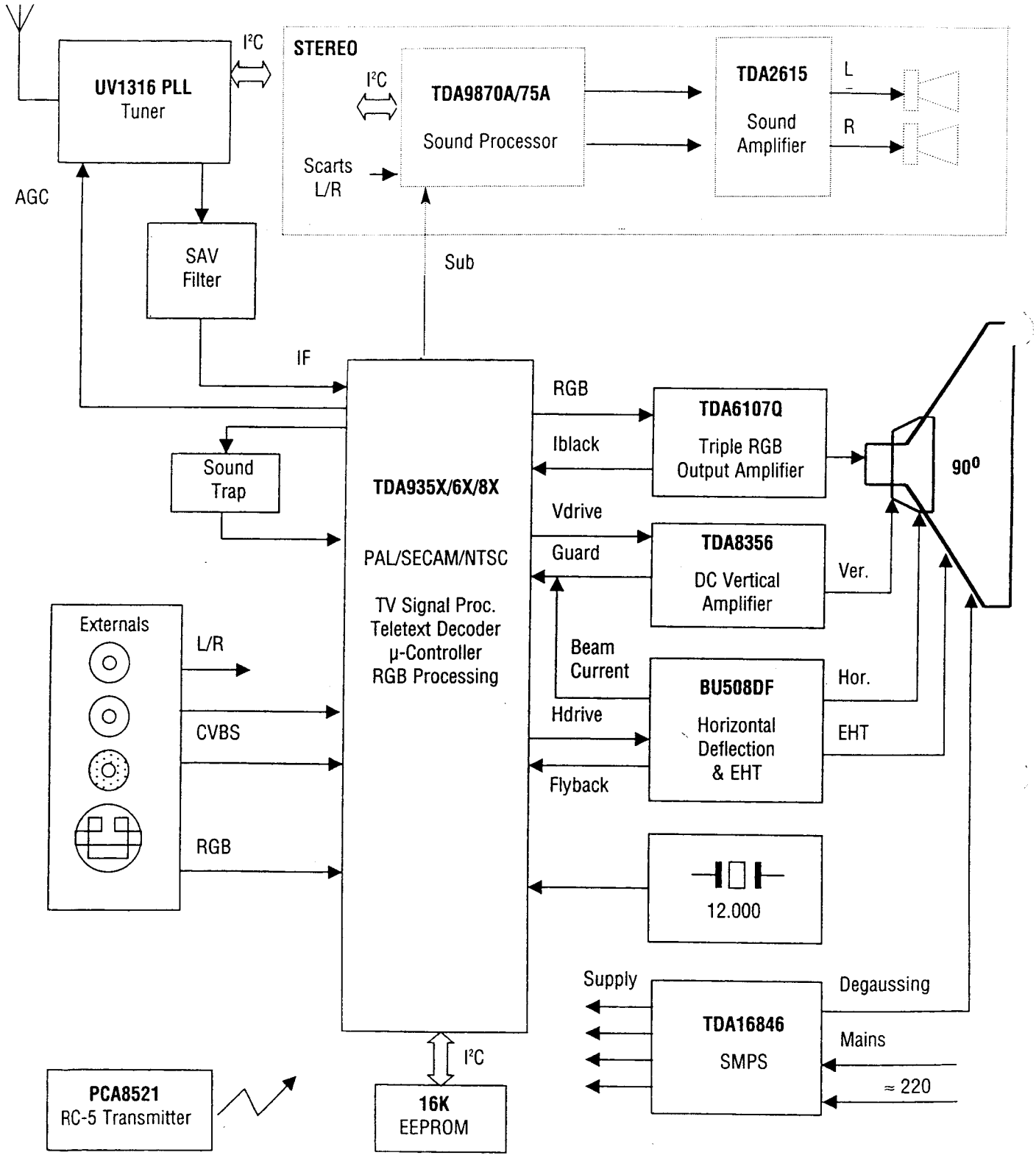
20" MEGA CTV

21" MEGA CTV

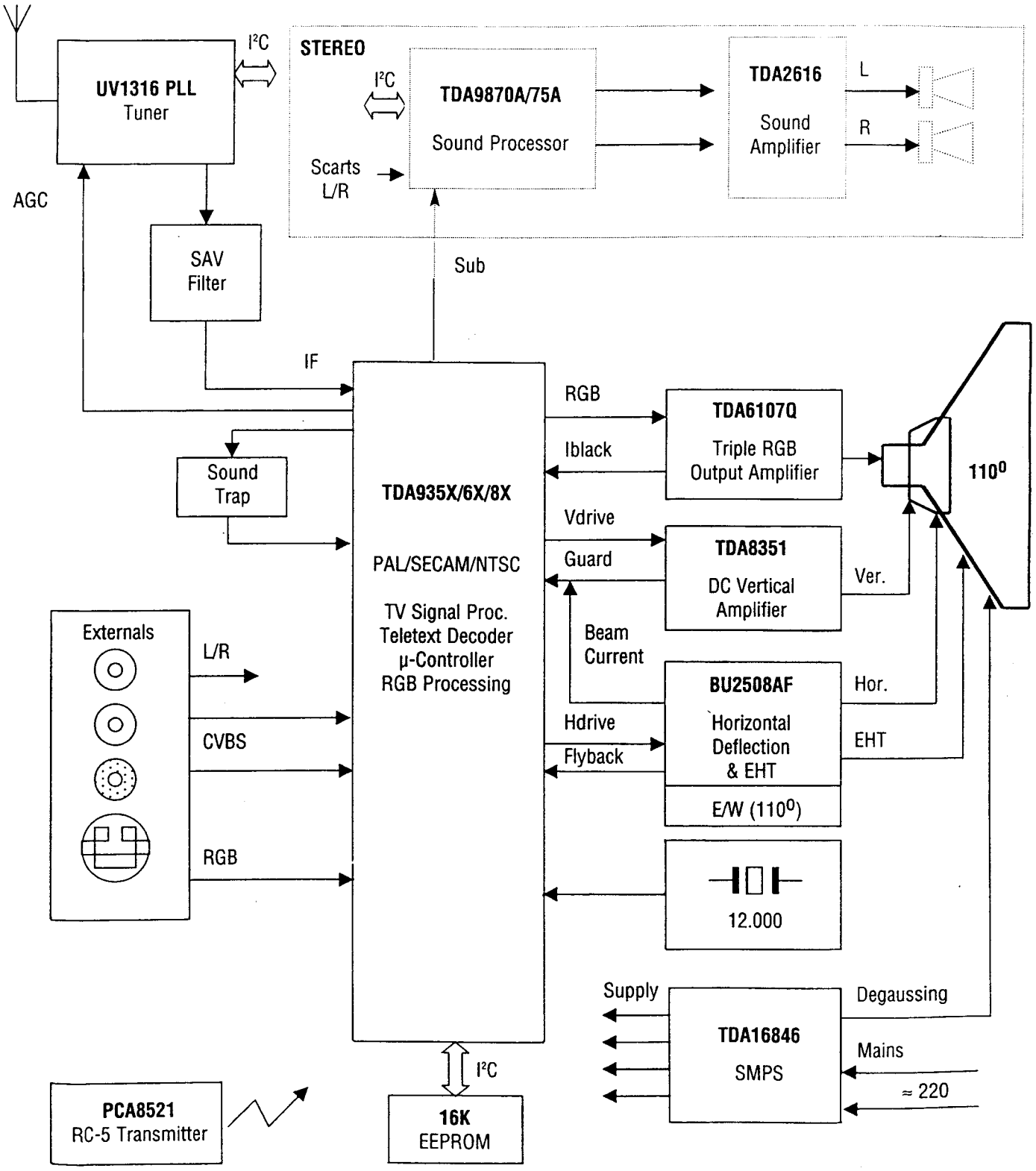
1- 21" MEGA CABINET
2- ACRYLIC WINDOW 21" CRT
3- 21" CRT
4- CRT SCREW Ø 7x30
5- SPEAKER
6- SPEAKER SCREW Ø 3.9x10
7- CRT RUBBER
8- MULTIPLE BUTTON
9- MULTIPLE BUTTON SCREW Ø 2.9x9.5
10- AV PCB
11- AV PCB HOLDER
12- AV HOLDER SCREW Ø 2.9x9.5
13- POWER CABLE HOLDER
14- POWER CABLE
15- LOGO PCB
16- LOGO ACR.
17- LOGO
18- MAIN PCB
19- ON-OFF BUTTON
20- CRT PCB
21- BACK COWER
22- BACK COWER SCREW Ø 3.9x19
23- BACK COWER LABEL
24- FRONT FRAME



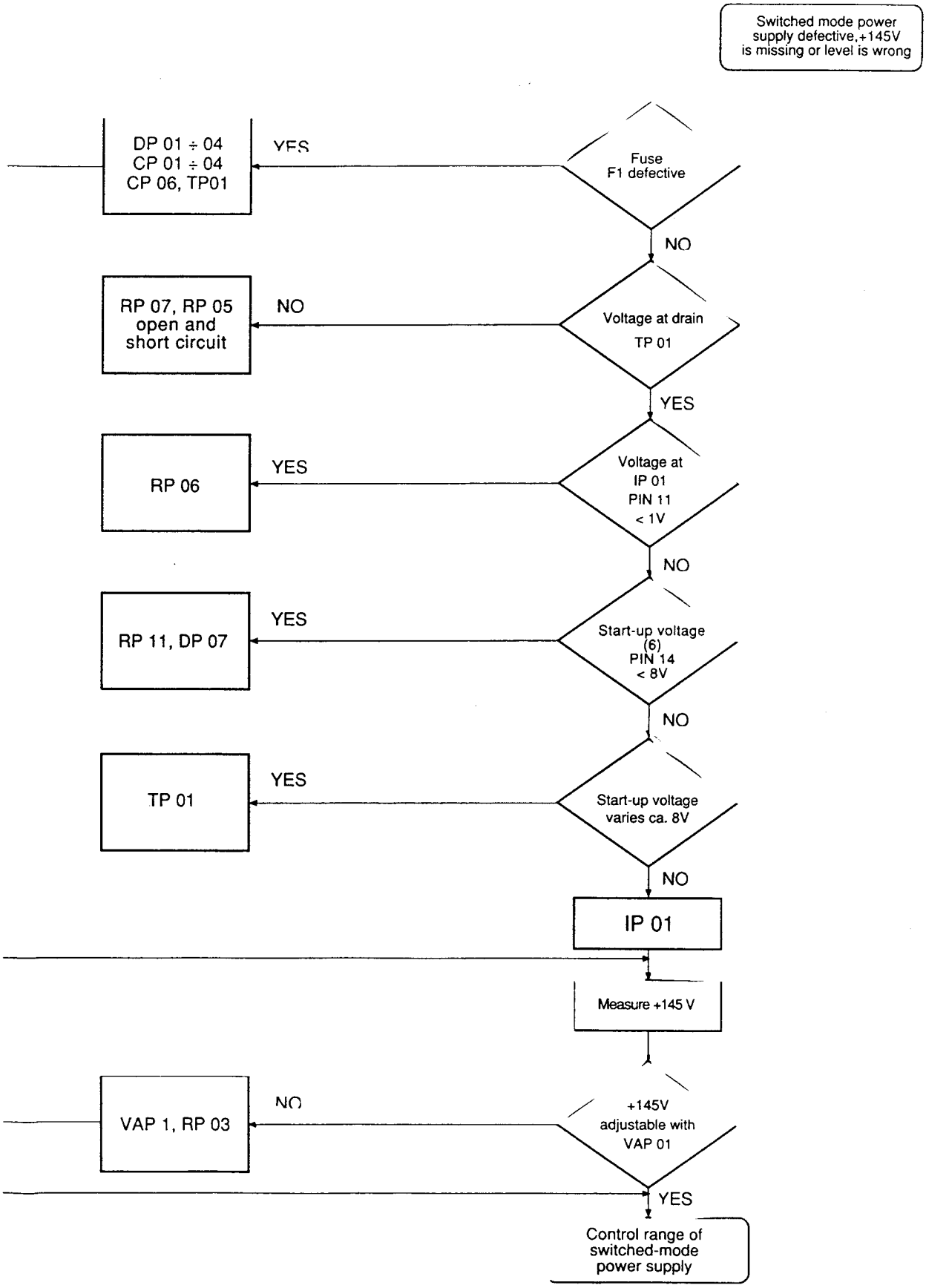
PT92 90° STEREO CHASSIS



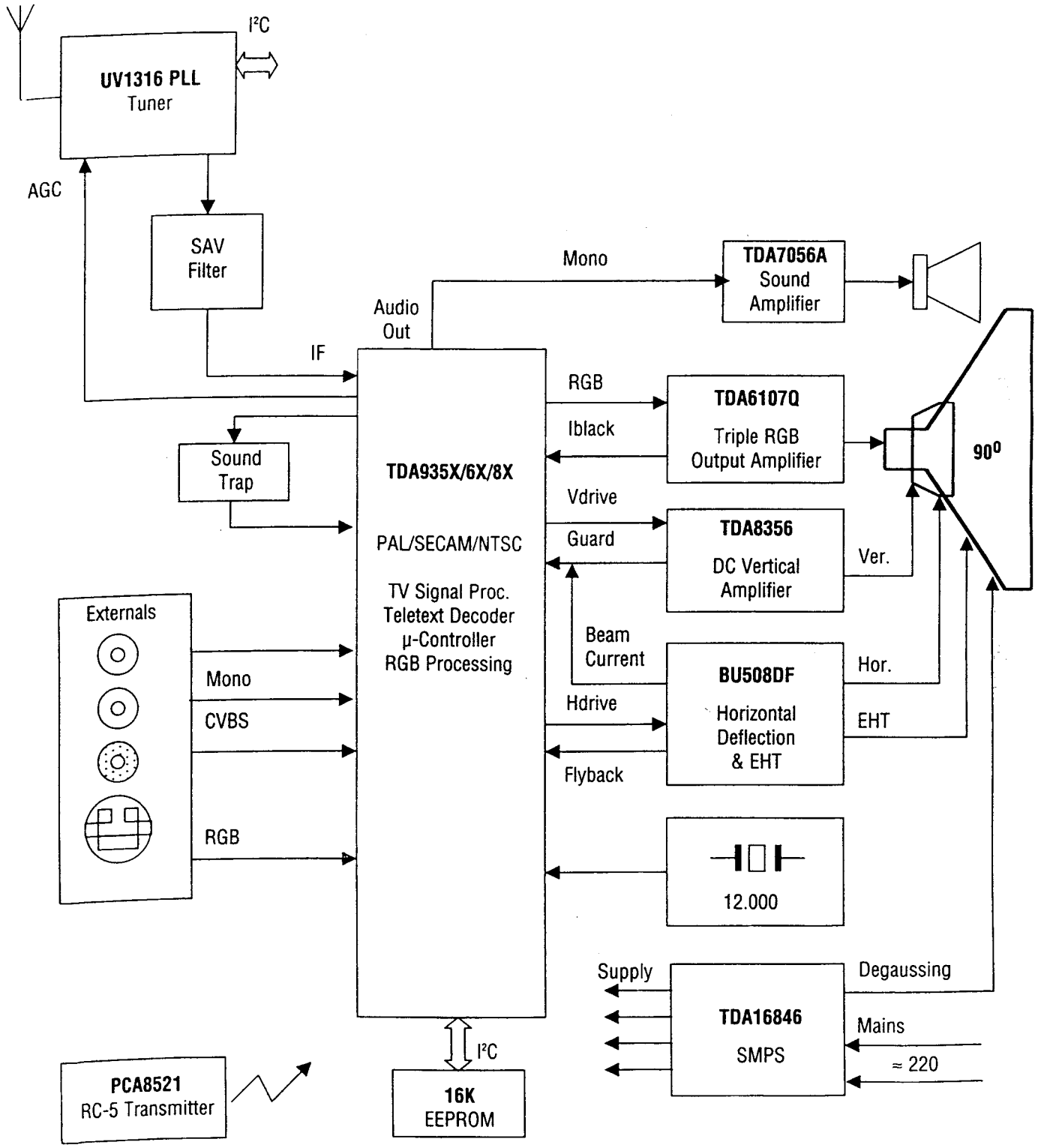
PT92 110° STEREO CHASSIS



FAULT TRACING DIAGRAM-POWER SUPPLY

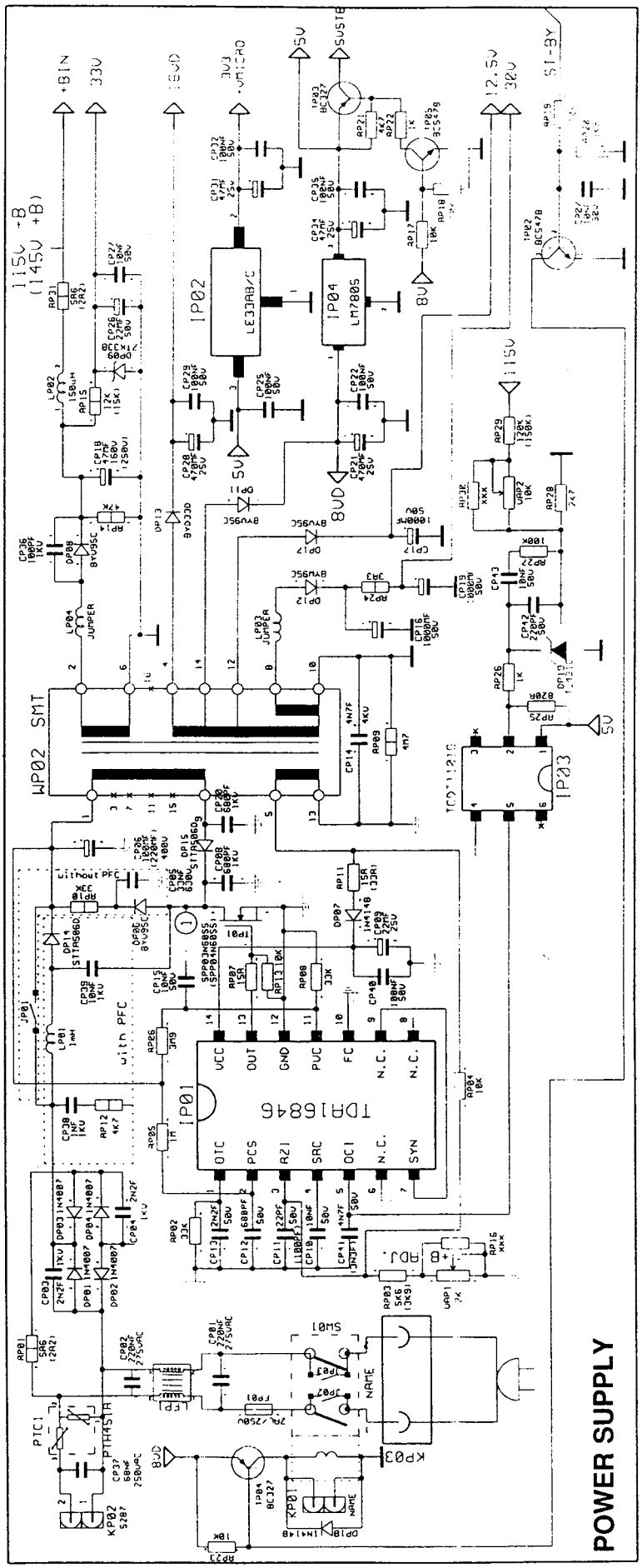


PT92 90° MONO CHASSIS

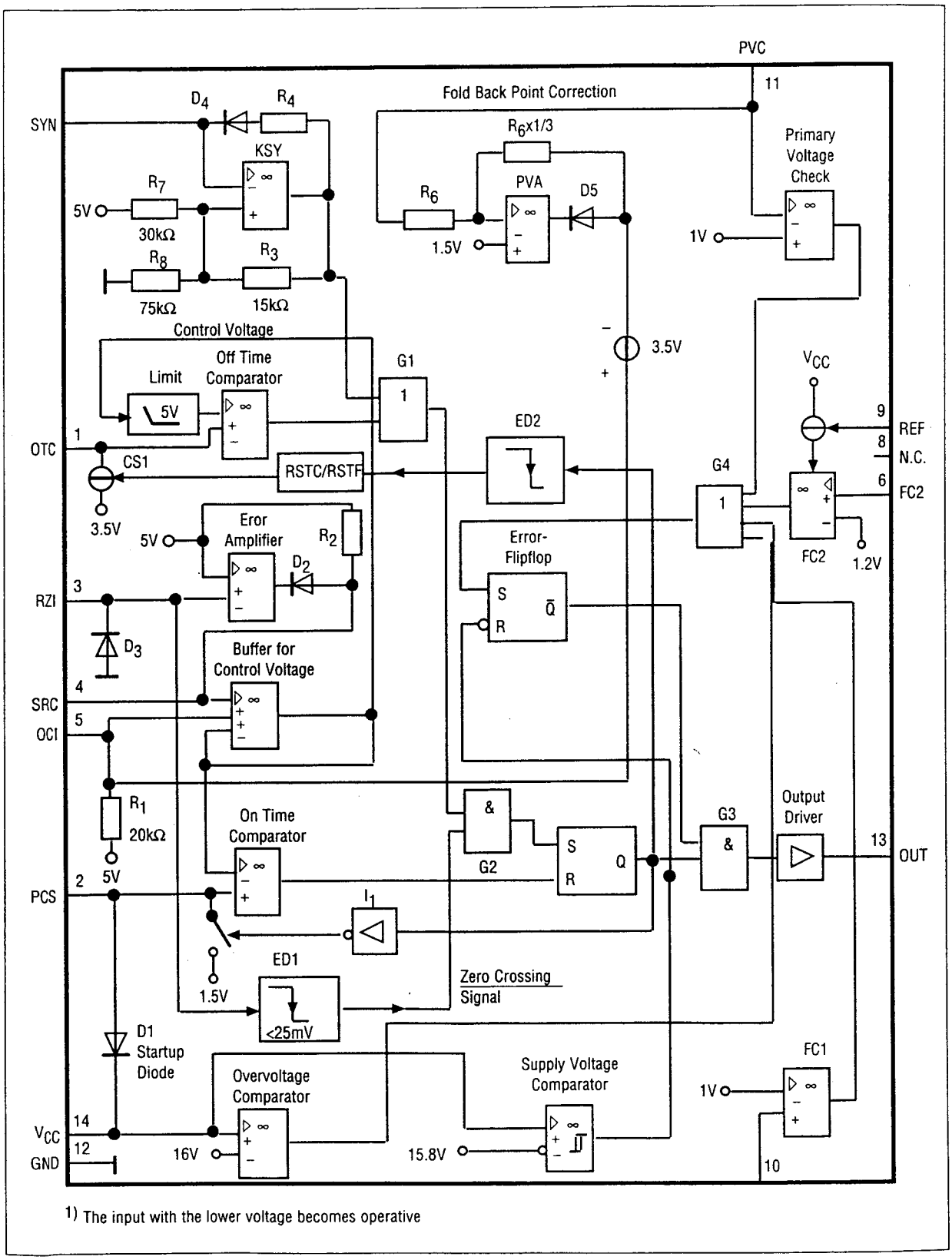


TROUBLESHOOTING GUIDE FOR MAIN PCB

TROUBLE	CHECK POINTS
No color	CV37, CV38, XV01
Horizontal linearity	LD02, RD20, DD06
Horizontal size	+B voltage, CD18, CD20, CD27, CD08, TV06
Flue picture	RD17, RD06, RD62, R001, Focus adjust
Dark picture	Screen adjust, EHT voltage
Noise picture	TU01, AGC adjust, If adjust
Interference	TV01, TV04, TU01
No sound	IA50, IA51, IA01, DP17, DP12, RA51, X301, I302, IV01
Sound distortion	I302, IC01, L304, CA07, CA06, RA06, RA07, IA01, IA50, IA51
Memory	IC02, IV01, TC10
No video on the SCART	IV01, TE01, TE04
No audio on the SCART	I302, TV03
No picture	TD01, TD02, DD01, TD04, DD03, DD04, ID50, RD56, IV01


POWER SUPPLY
WP02 SMT
with PFC
without PFC
TDA16846
LE33AB/C
LM7805
115V -B
(145V +B)
+BIN
33V
8VD
5V
SUSTB
12.5V
32V
ST-BY
3V3 u-micro
JUMPER
NAME

TDA16846 Block Diagrams

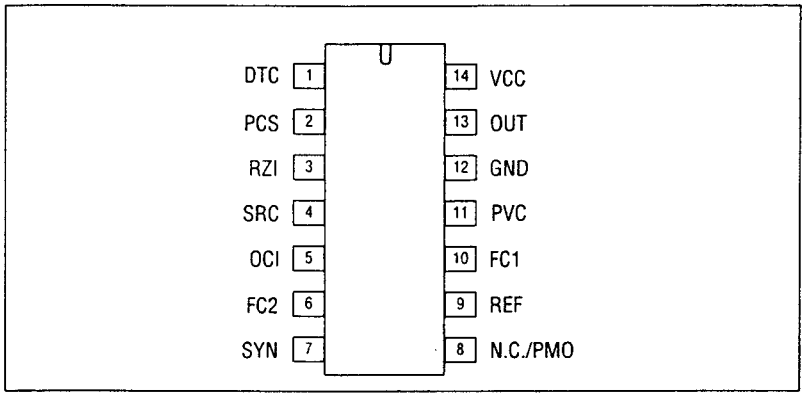


1) The input with the lower voltage becomes operative

TDA16846
Controller For Switch Mode Power Supplies

The TDA16846 is suited for TV-, VCR-sets and SAT receivers. It also can be good used in PC monitors.
The TDA 16847 is identical with TDA16846 but has an additional power measurement output (pin 8) which can be used a Temporary High Power Circuit.

Pin Configuration (top view)



Pin Definitions and Functions

Pin	Symbol	Function
1	OTC	Off Time Circuit
2	PCS	Primary Current Simulation
3	RZI	Regulation and Zero Crossing Input
4	SRC	Soft-Start and Regulation Capacitor
5	OCI	Opto Coupler Input
6	FC2	Fault Comparator 2
7	SYN	Synchronization Input
8	N.C./PMO	Not Connected (TDA16846)
9	REF	Reference Voltage and Current
10	FC1	Fault Comparator 1
11	PVC	Primary Voltage Check
12	GND	Ground
13	OUT	Output
14	VCC	Supply Voltage

Short Description of the Pin Functions

Pin	Functions
1	A parallel RC-circuit between this pin and ground determines the ringing suppression time and the standby-frequency.
2	A capacitor between this pin and ground and a resistor between this pin and the positive terminal of the primary elcap quantifies the max. possible output power of the SMPS.
3	This is the input of the error amplifier and the zero crossing input. The output of a voltage divider between the control winding and ground is connected to this input. If the pulses at pin 3 exceed a 5 V threshold, the control voltage at pin 4 is lowered.
4	This is the pin for the control voltage. A capacitor has to be connected between this pin and ground. The value of this capacitor determines the duration of the softstart and the speed of the control.
5	If an opto coupler for the control is used, it's output has to be connected between this pin and ground. The voltage divider at pin 3 has then to be changed, so that the pulses at pin 3 are below 5 V.
6	Fault comparator 2: If a voltage > 1.2 V is applied to this pin, the SMPS stops.
7	If fixed frequency mode is wanted, a parallel RC circuit has to be connected between this pin and ground. The RC-value determines the frequency. If synchronized mode is wanted, sync pulses have to be fed into this pin.
8	Not connected (TDA16846). / This is the power measurement output of the Temporary High Power Circuit. A capacitor and a RC-circuit has to be connected between this pin and ground.
9	Output for reference voltage (5 V). With a resistor between this pin and ground the fault comparator 2 (pin 6) is enabled.
10	Fault comparator i: If a voltage > 1 V is applied to this pin, the SMPS stops.
11	This is the input of the primary voltage check. The voltage at the anode of the primary elcap has to be fed to this pin via a voltage divider. If the voltage of this pin falls below 1 V, the SMPS is switched off. A second function of this pin is the primary voltage dependent fold back point correction (only active in free running mode).
12	Common ground.
13	Output signal. This pin has to be connected across a serial resistor with the gate of the power transistor.
14	Connection for supply voltage and startup capacitor. After startup the supply voltage is produced by the control winding of the transformer and rectified by an external diode.

ELECTRICAL CHARACTERISTICS

Absolute maximum ratings

All voltages listed are referenced to ground (0V, Vss) except where noted.

Parameter	Symbol	Limit Values		Unit	Remarks
		Min.	Typ.		
Supply Voltage at Pin 14	V_{CC}	-0.3	17	V	-
Voltage at Pin 1, 4, 5, 6, 7, 9, 10	-	-0.3	6	V	-
Voltage at Pin 2, 8, 11	-	-0.3	17	V	-
Voltage at Pin 3	RZI		6	V	-
Current into Pin 3		-10		mA	$V_3 < -0.3V$
Current into Pin 9	REF	-1	-	mA	-
Current into Pin 13	OUT		100	mA	$V_{13} > -V_{CC}$
		-100		mA	$V_{13} < -0V$
ESD Protection	-	-	2	kV	MIIL STD 883C methot 3015.6, 100 PF, 1500Ω
Storage Temperature	T_{stg}	-65	125	°C	-
Operating Junction Temperature	T_j	-	125	°C	-
Thermal Resistance Junction-Ambient	R_{thJA}	-	110	K/W	P-DIP-14-3
Soldering Temperature	-	-	260	°C	-
Soldering Time -	-	10	s	-	

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

µ-CONTROLLER

- 80C51 µ-controller core standard instruction set and timing
- 1 µs machine cycle
- 32 - 128Kx8-bit late programmed ROM
- 3 - 12Kx8-bit Auxiliary RAM (shared with Display and Acquisition)
- Interrupt controller for individual enable/disable with two level priority
- Two 16-bit Timer/Counter registers
- WatchDog timer
- Auxiliary RAM page pointer
- 16-bit Data pointer
- IDLE and Power Down (PD) mode
- 14 bits PWM for Voltage Synthesis Tuning
- 8-bit A/D converter
- 4 pins which can be programmed as general I/O pin, ADC input or PWM (6-bit) output

DATA CAPTURE

- Text memory for 1 or 10 pages
- In the 10 page versions inventory of transmitted Teletext pages stored in the Transmitted Page Table (TPT) and Subtitle Page Table (SPT)
- Data Capture for US Closed Caption
- Data Capture for 525/625 line WST, VPS (PDC system A) and Wise Screen Signalling (WSS) bit decoding
- Automatic selection between 525 WST/625 WST
- Automatic selection between 625 WST/VPS on line 16 of VBI
- Real-time capture and decoding for WST Teletext in Hardware, to enable optimized µ-processor throughput
- Automatic detection of FASTEXT transmission
- Real-time packet 26 engine in Hardware for processing accented, G2 and G3 characters
- Signal quality detector for video and WST/VPS data types
- Comprehensive teletext language coverage
- Full Field and Vertical Blanking Interval (VBI) data capture of WST data

DISPLAY

- Teletext and Enhanced OSD modes
- Features of level 1.5 WST and US Close Caption
- Serial and Parallel Display Attributes
- Single/Double/Quadruple Width and Height for characters
- Scrolling of display region
- Variable flash rate controlled by software
- Enhanced display features including overlining, underlining and italics
- Soft colours using CLUT with 4096 colour palette
- Globally selectable scan lines per row (9/10/13/16) and character matrix [12x10, 12x13, 12x16 (VxH)]
- Fringing (Shadow) selectable from N-S-E-W direction
- Fringe colour selectable
- Meshing of defined area
- Contrast reduction of defined area
- Cursor
- Special Graphics Characters with two planes, allowing four colours per character
- 32 software redefinable On-Screen display characters
- 4 WST Character sets (GO/G2) in single device (e.g. Latin, Cyrillic, Greek, Arabic)
- G1 Mosaic graphics, Limited G3 Line drawing characters
- WST Character sets and Closed Caption Character set in single device.

TDA935X/6X/8X
TV signal processor-Teletext decoder with embedded μ-Controller

GENERAL DESCRIPTION

The various versions of the TDA935X/6X/8X series combine the functions of a n/ signal processor together with a μ-Controller and US Closed Caption decoder. Most versions have a Teletext decoder on board. The Teletext decoder has an internal RAM memory for 1 or 10 page text. The ICs are intended to be used in economy television receivers with 90° and 110° picture tubes.

The ICs have supply voltages of 8 V and 3.3 V and they are mounted in S-DIP envelope with 64 pins.

The features are given in the following feature list. The differences between the various ICs are given in the table on page 4.

FEATURES

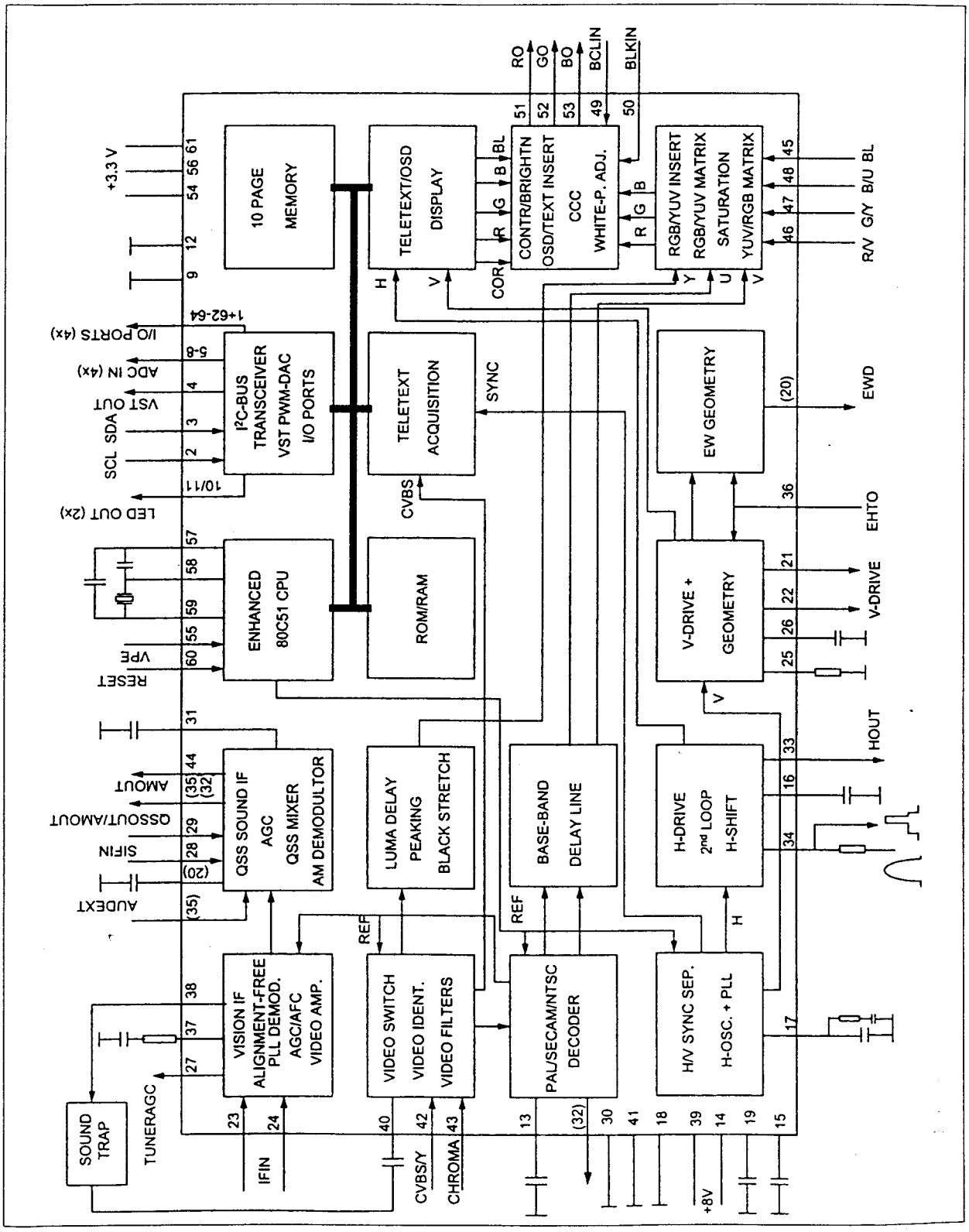
TV-signal processor

- Multi-standard vision IF circuit with alignment-free PLL demodulator
- Internal (switchable) time-constant for the IF-AGC circuit
- A choice can be made between versions with mono intercarrier sound FM demodulator and versions with QSS IF amplifier.
- The mono intercarrier sound versions have a selective FM-PLL demodulator which can be switched to the different FM sound frequencies (4.5/5.5/6.0/6.5 MHz). The quality of this system is such that the external band-pass filters can be omitted.
- Source selection between 'internal' CVBS and external CVBS or Y/C signals
- Integrated chrominance trap circuit
- Integrated luminance delay line with adjustable delay time
- Asymmetrical 'delay line type' peaking in the luminance channel
- Black stretching for non-standard luminance signals
- Integrated chroma band-pass filter with switchable centre frequency
- Only one reference (12 MHz) crystal required for the CL-Controller, Teletext- and the colour decoder
- PAL/NTSC or multi-standard colour decoder with automatic search system
- Internal base-band delay line
- RGB control circuit with 'Continuous Cathode Calibration', white point and black level off set adjustment so that the colour temperature of the dark and the light parts of the screen can be chosen independently.
- Linear RGB or YUV input with fast blanking for external RGB/YUV sources. The Text/OSD signals are internally supplied from the μ-Controller/Teletext decoder
- Contrast reduction possibility during mixed-mode of OSD and Text signals
- Horizontal synchronization with two control loops and alignment-free horizontal oscillator
- Vertical count-down circuit
- Vertical driver optimized for DC-coupled vertical output stages
- Horizontal and vertical geometry processing
- Horizontal and vertical zoom function for 16 : 9 applications
- Horizontal parallelogram and bow correction for large screen picture tubes

QUICK REFERENCE DATA

SYMBOL	PARAMETER	Min.	Typ.	Max.	Unit
Supply					
V_P	supply voltage	-	8.0/3.3	-	V
I_p	supply current	-	tbf	-	mA
Input voltages					
$V_{iSIF(rms)}$	video IF amplifier sensitivity (RMS value)	-	35	-	µV
$V_{iVIF(rms)}$	QSS sound IF amplifier sensitivity (RMS value)	-	60	-	µV
$V_{iAUDIO(rms)}$	external audio input (RMS value)	-	500	-	mV
$V_{iCVBS(p-p)}$	external CVBS/Y input (peak-to-peak value)	-	1.0	-	V
$V_{iCHORAMA(p-p)}$	external chroma input voltage (burst amplitude) (peak-to-peak value)	-	0.3	-	V
$V_{iRGB(p-p)}$	RGB inputs (peak-to-peak value)	-	0.7	-	V
$V_{iYIN(p-p)}$	luminance input signal (peak-to-peak value)	-	1.4	-	V
$V_{iUVIN(p-p)}$	U/V input signal (peak-to-peak value)	-	1.33/1.05	-	V
Output signals					
$V_{o(IFVO(p-p)}$	demodulated CVBS output (peak-to-peak value)	-	2.5	-	V
$V_{o(QSSO)(rms)}$	sound IF intercarrier output in QSS versions (RMS value)	-	100	-	mV
$V_{o(AMOUT)(rms)}$	demodulated AM sound output in QSS versions (RMS value)	-	500	-	mV
$I_{o(AGCOUT)}$	tuner AGC output current range	0	-	5	mV
$V_{oRGB(p-p)}$	RGB output signal amplitudes (peak-to-peak value)	-	2.0	-	V
$I_{o\ HOUT}$	horizontal output current	10	-	-	mA
$I_{o\ VERT}$	vertical output current (peak-to-peak value)	1	-	-	mA
$I_{o\ EWD}$	EW drive output current	1.2	-	-	mA

Block Diagram



PINNING

SYMBOL	PIN	DESCRIPTION
GND1	41	ground 1 for TV-processor
CVBS/Y	42	external CVBS/Y input
CHROMA	43	chrominance input (SVHS)
AUDOUT / AMOUT [1]	44	audio output / AM audio output (volume controlled)
INSSW2	45	2nd RGB /YUV insertion input
R2/VIN	46	2nd R input / V (R-Y) input
G2 YIN	47	2nd G input Y input
B2 UIN	48	2nd B input / U (B-Y) input
BCLIN	49	beam current limiter input/V-guard input
BLKIN	50	black current input
RO	51	Red output
GO	52	Green output
BO	53	Blue output
VDDA	54	analog supply of Teletext decoder and digital supply of TV-processor (3.3 V)
VPE	55	OTP Programming Voltage
VDDC	56	digital supply to core (3.3V)
OSCGND	57	oscillator ground supply
XTALIN	58	crystal oscillator input
XTALOUT	59	crystal oscillator output
RESET	60	reset
VDDP	61	digital supply to periphery (+3.3 V)
P1.0/INT1	62	port 1.0 or external interrupt 1 input
P1.1/T0	63	port 1.1 or Counter/Timer 0 input
P1.2/INT0	64	port 1.2 or external interrupt 0 input

Note

1. The function of pin 20, 28, 29, 31, 32, 35 and 44 is dependent on the IC version (mono intercarrier FM demodulator / QSS IF amplifier and East-West output or not) and on some software control bits. The valid combinations are given in table 1.

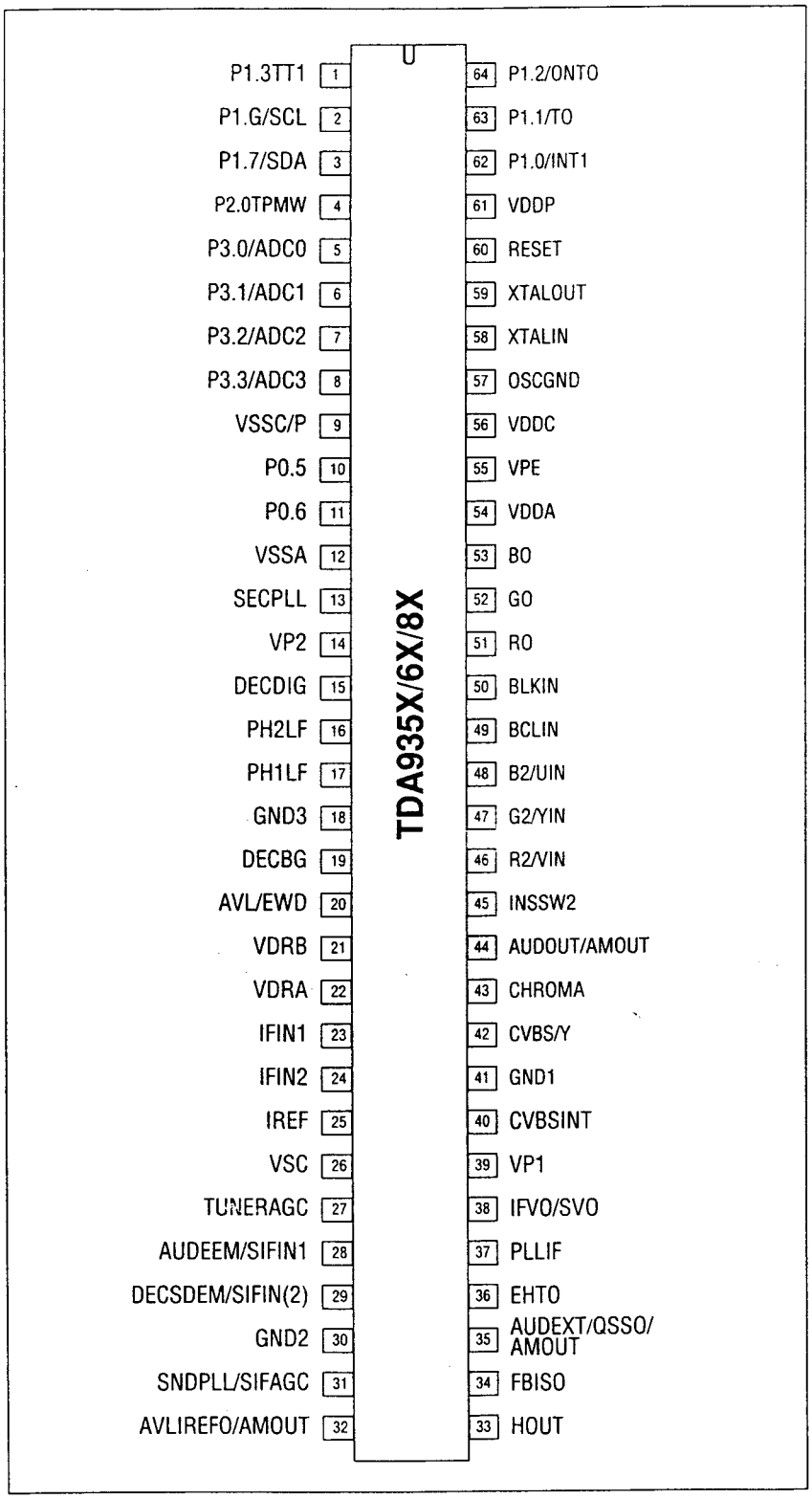
Table 1 Pin functions for various versions

IC version	FM-PLL version			QSS version					
East-West Y/N	N	Y		N			Y		
CMB1/CMB0 bits	-	00	01/10/11	00	01/10/11		00	01/10/11	
AM bit	-	-	-	-	0	1	-	0	1
Pin 20	AVL	EWD		AVL			EWD		
Pin 28	AUDEEM			SIFIN1					
Pin 29	DECSDEM			SIFIN2					
Pin 31	SNDPLL			SIFAGC					
Pin 32	REFO	AVL	REFO	AMOUT	REFO		AMOUT	REFO	
Pin 35	AUDEXT			AUDEX	QSSO	AMOUT	AUDEXT	QSSO	AMOUT
Pin 44	AUDOUT			controlled AM out					

PINNING

SYMBOL	PIN	DESCRIPTION
P1.3TT1	1	port 1.3 or Counter/Timer 1 input
P1.6/SCL	2	port 1.6 or I²C-bus clock line
P1.7/SDA	3	port 1.7 or I²C-bus data line
P2. O/TPWM	4	port 2.0 or Tuning PWM output
P3.0/ADC0	5	port 3.0 or ADC0 input
P3.1/ADCI	6	port 3.1 or ADC1 input
P3.2/ADC2	7	port 3.2 or ADC2 input
P3.3/ADC3	8	port 3.3 or ADC3 input
VSSC/P	9	digital ground for µ-Controller core and periphery
P0.5	10	port 0.5 (8 mA current sinking capability for direct drive of LEDs)
P0.6	11	port 0.6 (8 mA current sinking capability for direct drive of LEDs)
VSSA	12	analog ground of Teletext decoder and digital ground of TV- processor
SECPLL	13	SECAM PLL decoupling
VP2	14	2nd supply voltage TV-processor (+8V)
DECDIG	15	decoupling digital supply of TV-processor
PH2LF	16	phase-2 filter
PH1LF	17	phase-1 filter
GND3	18	ground 3 for TV-processor
DECBG	19	bandgap decoupling
AVL/EWD(1)	20	Automatic Volume Levelling /East-West drive output
VDRB	21	vertical drive B output
VDRA	22	vertical drive A output
IFIN1	23	IF input 1
IFIN2	24	IF input 2
IREF	25	reference current input
VSC	26	vertical sawtooth capacitor
TUNERAGC	27	tuner AGC output
AUDEEM/SIFIN1(1)	28	audio deemphasis or SIF input 1
DECSDEM/SIFIN2(1)	29	decoupling sound demodulator or SIF input 2
GND2	30	ground 2 for TV-processor
SNDPLL/SIFAGC(1)	31	narrow band PLL filter / AGC sound IF
AVL/REF0/AMOUT(1)	32	Automatic Volume Levelling / subcarrier reference output/AM output (non controlled)
HOUT	33	horizontal output
FBISO	34	flyback input/sandcastle output
AUDEXT/ QSSO/AMOUT(1)	35	external audio input/QSS intercarrier out /AM audio output (non controlled)
EHTO	36	EHT/overvoltage protection input
PLLIF	37	IF-PLL loop filter
IFVO/SVO	38	IF video output / selected CVBS output
VP1	39	main supply voltage TV-processor (+8 V)
CVBSINT	40	internal CVBS input

Pin configuration (SDIP 64)



TDA9870A
Digital TV sound processor (DTVSP)

FEATURES

1.1 Demodulator and decoder section

- Sound IF (SIF) input switch e.g. to select between terrestrial TV SIF and SAT SIF sources
- SIF AGC with 24 dB control range
- SIF 8-bit Analog-to-Digital Converter (ADC)
- Two-carrier multistandard FM demodulation (B/G, D/K and M standard)
- Decoding for three analog multi-channel systems (A2, A2+ and A2*) and satellite sound
- Programmable identification (B/G, D/K and M standard) and different identification times.

1.2 DSP section

- Digital crossbar switch for all digital signal sources and destinations
- Control of volume, balance, contour, bass, treble, pseudo stereo, spatial, bass boost and soft-mute
- Plop-free volume control
- Automatic Volume Level (AVL) control
- Adaptive de-emphasis for satellite
- Programmable beeper
- Monitor selection for FM/AM DC values and signals, with peak detection option
- I^2S-bus interface for a feature extension (e.g. Dolby surround) with matrix, level adjust and mute.

1.3 Analog audio section

- Analog crossbar switch with inputs for mono and stereo (also applicable as SCART 3 input), SCART 1 input/output, SCART 2 input/output and line output
- User defined full-level/-3 dB scaling for SCART outputs
- Output selection of mono, stereo, dual A/B, dual A or dual B
- 20 kHz bandwidth for SCART-to-SCART copies
- Standby mode with functionality for SCART copies
- Dual audio digital-to-analog converter from DSP to analog crossbar switch, bandwidth 15 kHz
- Dual audio ADC from analog inputs to DSP
- Two dual audio Digital-to-Analog Converters (DACs) for loudspeaker (Main) and headphone (Auxiliary) outputs; also applicable for L, R, C and S in the Dolby Pro Logic mode with feature extension.

2 GENERAL DESCRIPTION

The TDA9870A is a single-chip Digital TV Sound Processor (DTVSP) for analog multi-channel sound systems in TV sets and satellite receivers.

2.1 Supported standards

The multistandard/multi-stereo capability of the TDA9870A is mainly of interest in Europe, but also in Hong Kong/Peoples Republic of China and South East Asia.

This includes B/G, D/K, I, M and L standard. In other application areas there exists only subsets of those standard combinations otherwise only single standards are transmitted.

M standard is transmitted in Europe by the American Forces Network (AFN) with European channel spacing (7 MHz VHF, 8 MHz UHF) and monaural sound.

Korea has a stereo sound system similar to Europe and is supported by the TDA9870A. Differences include deviation, modulation contents and identification. It is based on M standard.

An overview of the supported standards and sound systems and their key parameters is given in.(Table 1).

The analog multi-channel sound systems (A2, A2+ and AP) are sometimes also named 2CS (2 carrier systems).

TV-Chassis PT-92 / 32"

stereo, 2 Scart, 16:9, CTV 481 ST/VT

TDA 9353PS/N1/2L0269
TDA 9353W2

IF	38,9
IFL1	33,4od.,9
HP	19
HB	32
EW	45
PW	13
UCP	9
LCP	13
TC	29
HP4:3	20
HB4:3	31
EW4:3	27
PW4:3	15
UCP4:3	13
LCP4:3	13
TC4:3	26
HS	24
VS	42
VA	45
SC	10
VSH	35
VX	25
BLR	9
BLG	8
WPR	52
WPG	36
WPB	32
Ys	5
Yn	5
Yp	5
Yo	5
AGC	20
CL	8
obige Werte können je nach Bildröhrentyp variieren	

Bits0	00	Opt3	6C
ACL	0		0
FCO	0	Jr	0
SVO	0	HP	1
HP2	0	Volbar	1
FSL	0	SubWoof	0
OSO	0	Presets	1
	0	Lock	1
	0	Hotel	0
Bits1	00	Opt4	B3
FFI	0	16:9	1
BTSC	0	110	1
FMWS	0	Hpol	0
BKS	0	Vpol	0
	0	Field	1
	0	Fe-Out	1
	0	Sw-on	0
	0	VG-Check	1
Opt1	01	Opt5	05
PAL-BG	1	Clock	1
PAL-DK	0	AM/PM	0
PAL-I	0	AVL	0
PAL-M	0		0
PAL-N	0	1-norma	0
NTSC-M	0		0
NTSC-443	0		0
SECAM-BG	0		0
Opt2	18	Opt6	00
SECAM-DK	0	UOC-J	0
FRANCE	0	ignrSUP	0
WEB	0	ignrNDF	0
PalBg Src	1		0
AV2	1	PAL-L	0
	0	Eco	0
	0	WEB St.	0
	0		0

Tunerwerte

TSL	045
TEL	118
TSM	118
TEM	400
TSH	400
TEH	863
TBL	01
TBM	06
TBH	85

TV-Chassis PT-92 / 14" bis 28" / 90° & 110° Ablenkung / Mono & Stereo
stereo, 2 Scart CTV 443ST/VT-P ab S/N 200004..., CTV 454 VT/ST

IF	38,9
IFL1	33,4
HP	31
HB	31
EW	46
PW	21
UCP	13
LCP	13
TC	28
HS	35
VS	42
VA	36
SC	3
VSH	25
VX	25
BLR	8
BLG	8
WPR	40
WPG	36
WPB	32
Ys	5
Yn	5
Yp	5
Yo	5
AGC	25
CL	11
obige Werte können je nach Bildröhrentyp variieren	

Bits0	00
ACL	0
FCO	0
SVO	0
HP2	0
TV	0
AV-1	0
AV-2	0
AV-2S	0
Bits1	00
AV-3	0
AV-3S	0
AV	0
WEB	0
NTSC-M	0
PAL-M	0
PAL-BG	0
	0
Opt1	FF
PAL-BG	1
PAL-DK	1
PAL-I	1
PAL-M	1
PAL-N	1
NTSC-M	1
NTSC-443	1
SECAM-BG	1
Opt2	1B
SECAM-DK	1
FRANCE	1
WEB	0
PalBg Src	1
AV2	1
	0
	0
	0

Tunerwerte

TSL	045
TEL	118
TSM	118
TEM	400
TSH	400
TEH	863
TBL	01
TBM	06
TBH	85

Opt3	68
	0
	0
HP	0
Volbar	1
SubWoof	0
Presets	1
Lock	1
Hotel	0

Opt4	B2	Opt5	09	Opt6	00
16:9	0	Clock	1	UOC-J	0
110	1	AM/PM	0	ignrSUP	0
Hpol	0	AVL	0	ignrNDF	0
Vpol	0		1		0
Field	1	1-norma	0		0
Fe-Out	1		0		0
Sw-on	0		0		0
VG-Check	1		0		0

TV-Chassis PT-92 / 14" bis 28" / 90° & 110° Ablenkung / Mono & Stereo

stereo, 1 Scart CTV 453 VT/ST

Bits0, Bits1, Opt1 + Opt2 können je nach Prozessor variieren

			TDA9350**S1** Init CTV832U 20/1		TDA9350**S2** Init CTV832U 21/4	
IF	38,9	Bits0	00	Bits0	00	
IFL1	33,4	ACL	0	ACL	0	
HP	31	FCO	0	FCO	0	
HB	31	SVO	0	SVO	0	
HS	31	HP2	0	HP2	0	
VS	40	TV	0	FSL	0	
VA	32	AV-1	0	OSO	0	
SC	14	AV-2	0		0	
VSH	30	AV-2S	0		0	
VX						
BLR	9	Bits1	00	Bits1	01	
BLG	7	AV-3	0	FFI	1	
WPR	43	AV-3S	0	BTSC	0	
WPG	42	AV	0	FMWS	0	
WPB	32	WEB	0	BKS	0	
Ys	5	NTSC-M	0		0	
Yn	5	PAL-M	0		0	
Yp	5	PAL-BG	0		0	
Yo	5		0		0	
AGC	25					
CL	11	Opt1	FF	Opt1	01 oder FF	
obige Werte können je nach Bildröhrentyp variieren		PAL-BG	1	PAL-BG	1	1
		PAL-DK	1	PAL-DK	0	1
		PAL-I	1	PAL-I	0	1
		PAL-M	1	PAL-M	0	1
		PAL-N	1	PAL-N	0	1
		NTSC-M	1	NTSC-M	0	1
		NTSC-443	1	NTSC-443	0	1
		SECAM-BG	1	SECAM-BG	0	1
Opt3	68	Opt2	0B	Opt2	08 oder 0B	
	0	SECAM-DK	1	SECAM-DK	0	1
	0	FRANCE	1	FRANCE	0	1
HP	0	WEB	0	WEB	0	0
Volbar	1	PalBg Src	1	PalBg Src	1	1
SubWoof	0	AV2	0	AV2	0	0
Presets	1		0		0	0
Lock	1		0		0	0
Hotel	0		0		0	0
Opt4	B0	Opt5	01	Opt6	00	
16:9	0	Clock	1	UOC-J	0	
110	0	AM/PM	0	ignrSUP	0	
Hpol	0	AVL	0	ignrNDF	0	
Vpol	0		0		0	
Field	1	1-norma	0		0	
Fe-Out	1		0		0	
Sw-on	0		0		0	
VG-Check	1		0		0	

Tunerwerte

TSL	045
TEL	118
TSM	118
TEM	400
TSH	400
TEH	863
TBL	01
TBM	06
TBH	85

TV-Chassis PT-92 / 14" bis 28" / 90° & 110° Ablenkung / Mono & Stereo

mono, 1 Scart CTV 426VT-N ab S/N 200004..., CTV 429VTP/4290VTP, 448, 450

Bits0, Bits1, Opt1 + Opt2 können je nach Prozessor variieren

			TDA9350**S1** Init CTV832U 20/1		TDA9350**S2** Init CTV832U 21/4	
IF	38,9	Bits0	00	Bits0	00	
IFL1	33,4	ACL	0	ACL	0	
HP	31	FCO	0	FCO	0	
HB	31	SVO	0	SVO	0	
HS	36	HP2	0	HP2	0	
VS	42	TV	0	FSL	0	
VA	57	AV-1	0	OSO	0	
SC	2	AV-2	0		0	
VSH	42	AV-2S	0		0	
VX						
BLR	9	Bits1	00	Bits1	01	
BLG	8	AV-3	0	FFI	1	
WPR	42	AV-3S	0	BTSC	0	
WPG	54	AV	0	FMWS	0	
WPB	32	WEB	0	BKS	0	
Ys	5	NTSC-M	0		0	
Yn	5	PAL-M	0		0	
Yp	5	PAL-BG	0		0	
Yo	5		0		0	
AGC	25					
CL	11	Opt1	FF	Opt1	01 oder FF	
obige Werte können je nach Bildröhrentyp variieren		PAL-BG	1	PAL-BG	1	1
		PAL-DK	1	PAL-DK	0	1
		PAL-I	1	PAL-I	0	1
		PAL-M	1	PAL-M	0	1
		PAL-N	1	PAL-N	0	1
		NTSC-M	1	NTSC-M	0	1
		NTSC-443	1	NTSC-443	0	1
		SECAM-BG	1	SECAM-BG	0	1
Opt3	68	Opt2	0B	Opt2	08 oder 0B	
	0	SECAM-DK	1	SECAM-DK	0	1
	0	FRANCE	1	FRANCE	0	1
HP	0	WEB	0	WEB	0	0
Volbar	1	PalBg Src	1	PalBg Src	1	1
SubWoof	0	AV2	0	AV2	0	0
Presets	1		0		0	0
Lock	1		0		0	0
Hotel	0		0		0	0
Opt4	B0	Opt5	01	Opt6	00	
16:9	0	Clock	1	UOC-J	0	
110	0	AM/PM	0	ignrSUP	0	
Hpol	0	AVL	0	ignrNDF	0	
Vpol	0		0		0	
Field	1	1-norma	0		0	
Fe-Out	1		0		0	
Sw-on	0		0		0	
VG-Check	1		0		0	

Tunerwerte

TSL	045
TEL	118
TSM	118
TEM	400
TSH	400
TEH	863
TBL	01
TBM	06
TBH	85

2.1.1 ANALOG 2-CARRIER SYSTEMS

Table 1 Frequency modulation

STANDARD	SOUND SYSTEM	CARRIER FREQUENCY (MHz)	FM DEVIATION (kHz) NOM./MAX./OVER	MODULATION		BANDWIDTH DE-EMPHASIS (kHz/µs)
				SC1	SC2	
M	mono	4.5	15/25/50	mono	-	15/75
M	A2+	4.5/4.724	15/25/50	1/2 (L + R)	1/2 (L - R)	15/75 (Korea)
B/G	A2	5.5/5.742	27/50/80	1/2 (L + R)	R	15/50
I	mono	6.0	27/50/80	mono	-	15/50
D/K	A2	6.5/6.742	27/50/80	1/2 (L + R)	R	15/50
D/K	A2*	6.5/6.258	27/50/80	1/2 (L + R)	R	15/50

Table 2 Identification for A2 systems

PARAMETER	A2/A2*	A2+ (KOREA)
Pilot frequency	54.6875 kHz = 3.5 x line frequency	55.0699 kHz = 3.5 x line frequency
Stereo identification frequency	117.5 Hz = $\frac{\text{line frequency}}{133}$	149.9 Hz = $\frac{\text{line frequency}}{105}$
Dual identification frequency	274.1Hz = $\frac{\text{line frequency}}{57}$	276.0 Hz = $\frac{\text{line frequency}}{57}$
AM modulation depth	50%	50%

2.1.2 SATELLITE SYSTEMS

An important for satellite TV reception is the 'Astra specification". The TDA9875A is suited for the reception of Astra and other satellite signals.

Table 3 FM satellite sound

CARRIER TYPE	CARRIER FREQUENCY (MHz)	MODULATION INDEX	MAXIMUM FM DEVIATION (kHz)	MODULATION	BANDWIDTH DE-EMPHASIS (kHz/µs)
main	6.50[1]	0.26	85	mono	15/50[1]
sub	7.02/7.20	0.15	50	m/st/d[2]	15/adaptive[3]
sub	7.38/7.56	0.15	50	m/st/d[2]	15/adaptive[3]
sub	7.74/7.92	0.15	50	m/st/d[2]	15/adaptive[3]
sub	8.10/8.28	0.15	50	m/st/d[2]	15/adaptive[3]

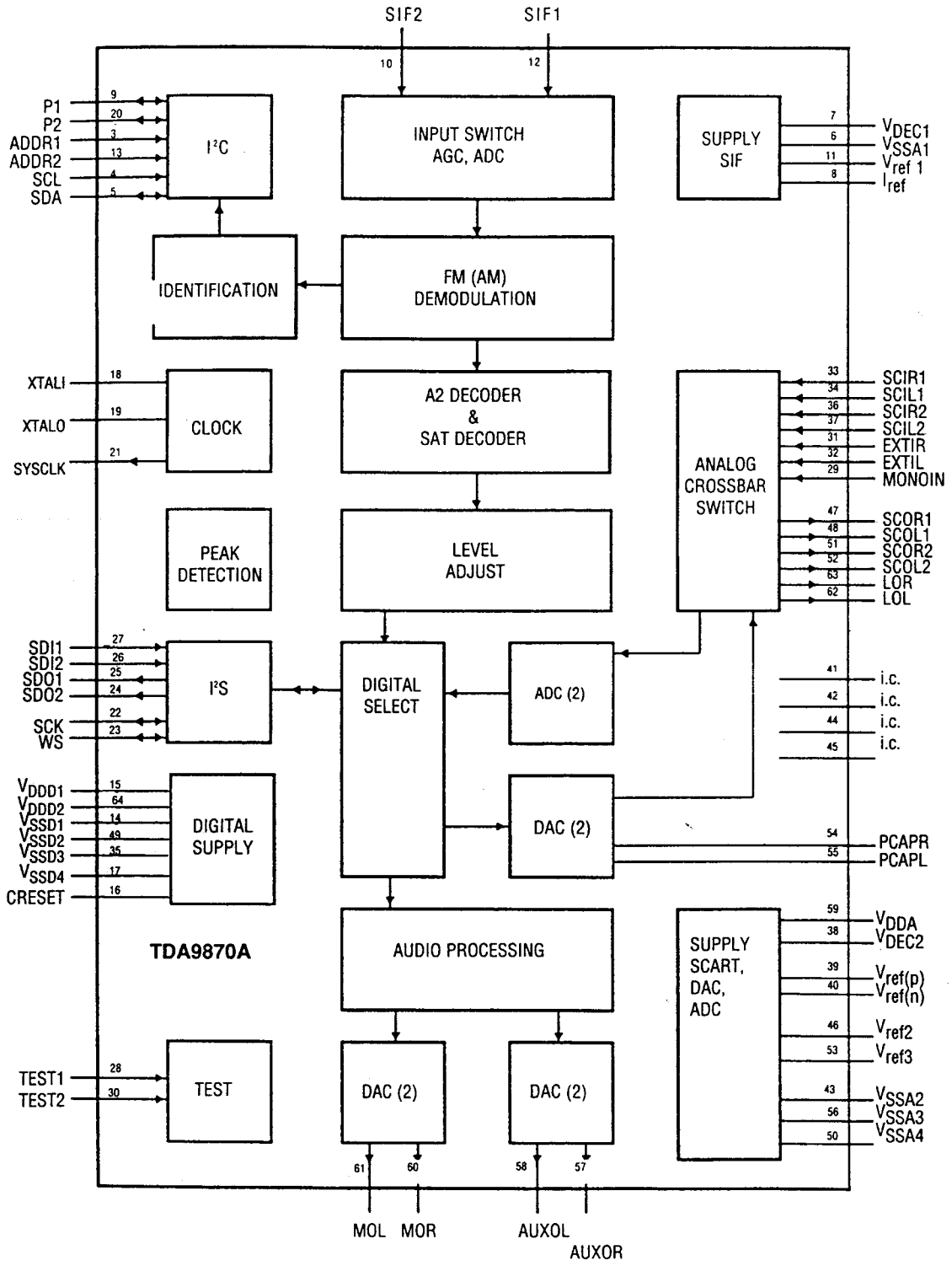
Notes

1. For other satellite systems, frequencies of, for example, 5.80, 6.60 or 6.65 MHz can also be received. A de-emphasis of 60 µs, or in accordance with J17, is available.
2. m/st/d = mono or stereo or dual language sound.
3. Adaptive de-emphasis = compatible to transmitter specification.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA9875A	SDIP64	plastic shrink dual-in-line package; 64 leads (750 mil)	SOT274-1

Block Diagram



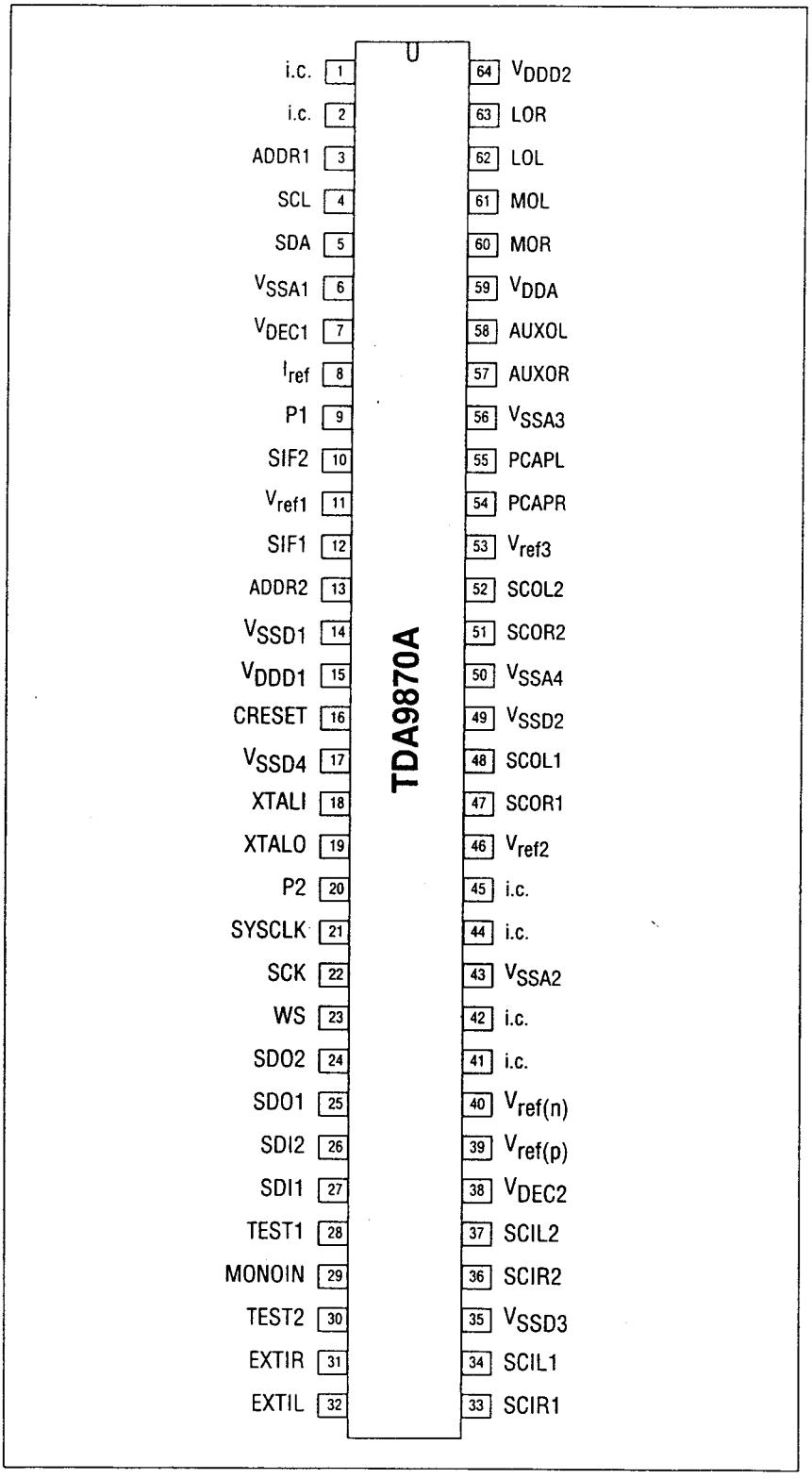
SYMBOL	PIN	I/O	DESCRIPTION
i.c.	1	-	internal connected; note 1
i.c.	2	-	internal connected; note 1
ADDR1	3	I	first I²C-bus slave address modifier
SCL	4	I	I²C-bus clock
SDA	5	I/O	I²C-bus data
V_{SSA1}	6	supply	supply ground 1; analog front-end circuitry
V_{DEC1}	7	-	positive power supply voltage 1 decoupling; analog front-end circuitry
I_{ref}	8	-	resistor for reference current generator; analog front-end circuitry
P1	9	I/O	first general purpose I/O pin
SIF2	10	-	sound IF input 2
V_{ref1}	11	-	reference voltage; analog front-end circuitry
SIF1	12	I	sound IF input 1
ADDR2	13	I	second I²C-bus slave address modifier
V_{SSD1}	14	supply	supply ground 1; digital circuitry
V_{DDD1}	15	supply	digital supply voltage 1; digital circuitry
CRESET	16	-	capacitor for power-on reset
V_{SSD4}	17	supply	supply ground 4; digital circuitry
XTALI	18	I	crystal oscillator input
XTALO	19	O	crystal oscillator output
P2	20	I/O	second general purpose I/O pin
SYSCLK	21	O	system clock output
SCK	22	I/O	I²C-bus clock
WS	23	I/O	I²C-bus word select
SDO2	24	O	I²C-bus data output 2
SDO1	25	O	I²C-bus data output 1
SDI2	26	I	I²C-bus data input 2
SDI1	27	I	I²C-bus data input 1
TEST1	28	I	first test pin; connected to V_{SSD1} for normal operation
MONOIN	29	I	audio mono input
TEST2	30	I	second test pin; connected to V_{SSD1} for normal operation
EXTIR	31	I	external audio input right channel
EXTIL	32	I	external audio input left channel
SCIR1	33	I	SCART 1 input right channel
SCIL1	34	I	SCART 1 input left channel
V_{SSD3}	35	supply	supply ground 3; digital circuitry
SCIR2	36	I	SCART 2 input right channel
SCIL2	37	I	SCART 2 input left channel
V_{DEC2}	38	-	positive power supply voltage 2 decoupling; audio analog to digital converter circuitry

SYMBOL	PIN	I/O	DESCRIPTION
$V_{ref(p)}$	39	-	positive reference voltage; audio analog to digital converter circuitry
$V_{ref(n)}$	40	-	reference voltage ground; audio analog-to-digital converter circuitry
i.c.	41	-	internally connected; note 2
i.c.	42	-	internally connected; note 3
V_{SSA2}	43	supply	supply ground; audio analog-to-digital converter circuitry
i.c.	44	-	internally connected; note 3
i.c.	45	-	internally connected; note 2
V_{ref2}	46	-	reference voltage; audio analog-to-digital converter circuitry
SCOR1	47	O	SCART 1 output right channel
SCOL1	48	O	SCART 1 output left channel
V_{SSD2}	49	supply	supply ground 2; digital circuitry
V_{SSA4}	50	supply	supply ground 4; audio operational amplifier circuitry
SCOR2	51	O	SCART 2 output right channel
SCOL2	52	O	SCART 2 output left channel
V_{ref3}	53	-	reference voltage; audio digital to analog converter and operational amplifier circuitry
PCAPR	54	-	post filter capacitor pin right channel, audio digital-to-analog converter
PCAPL	55	-	post filter capacitor pin left channel, audio digital-to-analog converter
V_{SSA3}	56	supply	supply ground 3; audio analog-to-digital converter circuitry
AUXOR	57	O	headphone (auxiliary) output right channel
AUXOL	58	O	headphone (auxiliary) output left channel
V_{DDA}	59	supply	positive analog power supply voltage; analog circuitry
MOR	60	O	loudspeaker (Main) output right channel
MOL	61	O	loudspeaker (Main) output left channel
LOL	62	O	line output left channel
LOR	63	O	line output right channel
V_{DDD2}	64	supply	digital supply voltage 2; digital circuitry

Notes

1. Test pin, CMOS 3-state stage, pull-up resistor, can be connected to V_{SS}.
2. Test pin, CMOS level input, pull-up resistor, can be connected to V_{SS}.
3. Test pin, CMOS 3-state stage, can be connected to V_{SS}.

Pin configuration



FUNCTIONAL DESCRIPTION

Description of the demodulator and decodersection

6.1.1 SIF INPUT

Two input pins are provided, SIF1 e.g. for terrestrial TV and SIF2 e.g. for a satellite tuner. For higher SIF signal levels the SIF input can be attenuated with an internal switchable -10 dB resistor divider. As no specific filters are integrated, both inputs have the same specification giving flexibility in application. The selected signal is passed through an AGC circuit and then digitized by an 8-bit ADC operating at 24.576 MHz.

6.1.2 AGC

The gain of the AGC amplifier is controlled from the ADC output by means of a digital control loop employing hysteresis The AGC has a fast attack behaviour to prevent ADC overloads and a slow decay behaviour to prevent AGC oscillations. For AM demodulation the AGC must be switched off. When switched off, the control loop is reset and fixed gain settings can be chosen (see table 14; subaddress 0).
The AGC can be controlled via the I²C-bus. Details can be found in the I²C-bus register definitions (see Chapter 10).

6.1.3 MIXER

The digitized input signal is fed to the mixers, which mix one or both input sound carriers down to zero IF. A 24-bit control word for each carrier sets the required frequency.
Access to the mixer control word registers is via the I²C-bus.

6.1.4 FM AND AM DEMODULATION

An FM or AM input signal is fed via a band-limiting filter to a demodulator that can be used for either FM or AM demodulation. Apart from the standard (fixed) de-emphasis characteristic, an adaptive de-emphasis is available for encoded satellite programs. A stereo decoder recovers the left and right signal channels from the demodulated sound carriers. Both the European and Korean stereo systems are supported.

6.1.5 FM AND AM DEMODULATION

The identification of the FM sound mode is performed by AM synchronous demodulation of the pilot signal and narrow-band detection of the identification frequencies. The result is available via the I²C-bus interface. A selection can be made via the I²C-bus for B/G, D/K and M standard and for three different modes that represent different trade-offs between speed and reliability of identification.

6.1.6 CRYSTAL OSCILLATOR

The crystal oscillator (XO) is illustrated in Fig.8 (see Chapter 12). The circuitry of the XO is fully integrated, only the external 24.576 MHz crystal is needed.

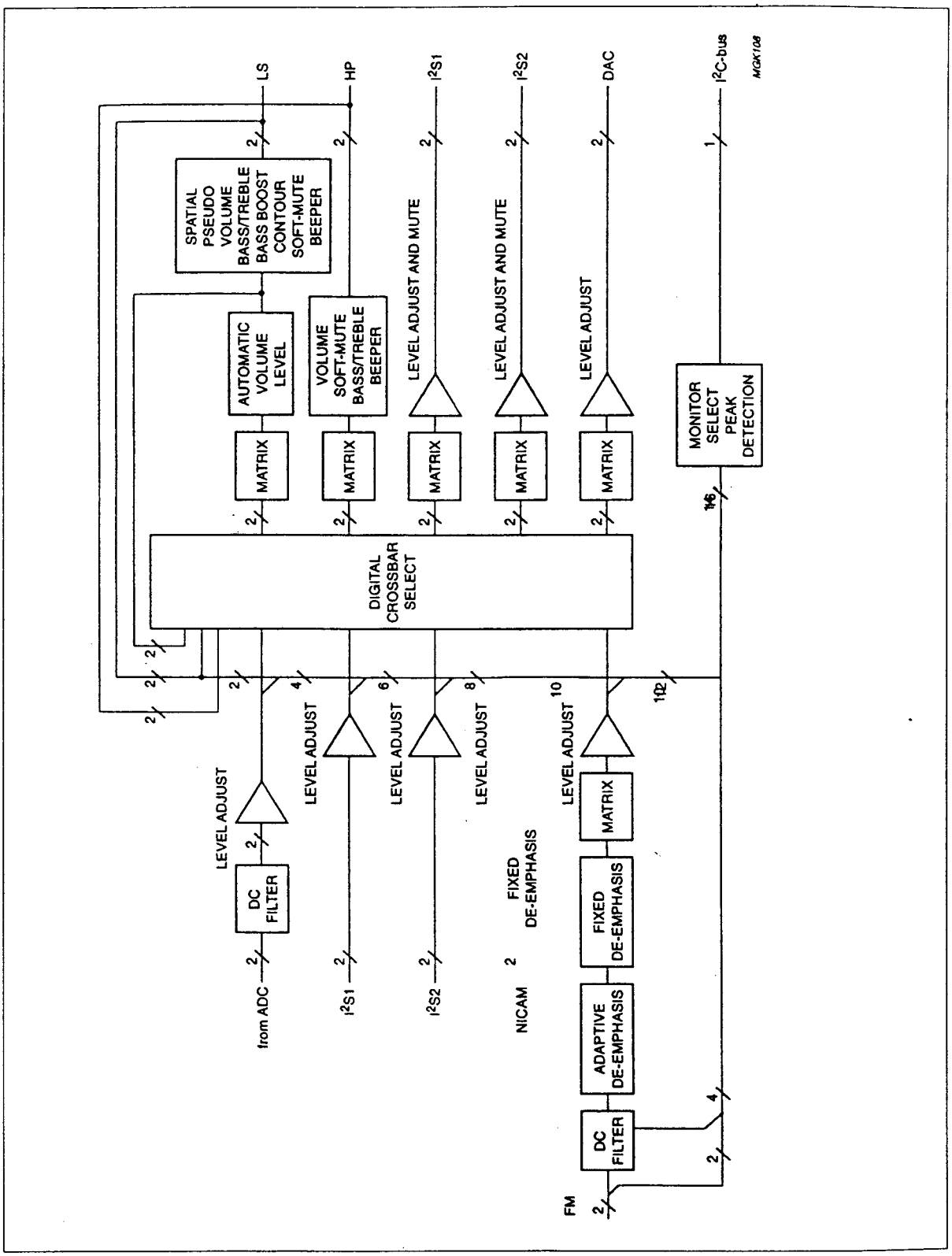
6.1.7 TEST PINS

Both test pins are active HIGH, in normal operation of the device they are wired to V_{SSD1}. Test functions are fo manufacturing tests only and are not available to customers. Without external circuitry these pads are pulled down to LOW level with internal resistors.

6.1.8 POWER-ON RESET FLIP-FLOP

The power-on reset flip-flop monitors the internal power supply for the digital part of the device. If the supply has temporary been lower than the specified lower limit, the power-on reset bit FOR, transmitter register subaddress O (see Section 10.4.1), will be set to HIGH. The CLRPOR bit, slave register subaddress 1 (see Section 10.3.2), resets the power-on reset flip-flop to LOW.

Description of the DSP



6.2.1 LEVEL SCALING

All input channels to the digital crossbar switch (except for the loudspeaker feedback path) are equipped with a level adjust facility to change the signal level in a range of ±15 dB. It is recommended to scale all input channels to be 15 dB below full scale (-15 dB full scale) under nominal conditions.

6.2.2 FM (AM) PATH

A high-pass filter suppresses DC offsets from the FM demodulator, due to carrier frequency offsets, and supplies the monitor/peak function with DC values and an unfiltered signal, e.g. for the purpose of carrier detection.

The de-emphasis function offers fixed settings for the supported standards (50 µs, 60 µs and 75 µs). An adaptive de-emphasis is available for Wegener-Panda 1 encoded programs.

A matrix performs the dematrixing of the A2 stereo, dual and mono signals.

6.2.3 MONITOR

This function provides data words from a number of locations of the signal processing paths to the I²C-bus interface (2 data bytes). Signal sources include the FM demodulator outputs, most inputs to the digital crossbar switch and the outputs of the ADC. Source selection and data read-out is performed via the I²C-bus.

Optionally, the peak value can be measured instead of simply taking samples. The internally stored peak value is reset to zero when the data is read via the I²C-bus. The monitor function may be used, for example, for signal level measurements or carrier detection.

6.2.4 LOUDSPEAKER (MAIN) CHANNEL

The matrix provides the following functions; forced mono, stereo, channel swap, channel 1, channel 2 and spatial effects.

There are fixed coefficient sets for spatial settings of 30%, 40% and 52%.

The Automatic Volume Level (AVL) function provides a constant output level of -23 dB full scale for input levels between 0 and -29 dB full scale. There are some fixed decay time constants to choose from, i.e. 2, 4 and 8 s.

Pseudo stereo is based on a phase shift in one channel via a 2nd-order all-pass filter. There are fixed coefficient sets to provide 90 degrees phase shift at frequencies of 150, 200 and 300 Hz.

Volume is controlled individually for each channel ranging from +24 to -83 dB with 1 dB resolution. There is also a mute position. For the purpose of a simple control software in the microcontroller, the decimal number that is sent as an I²C-bus data byte for volume control is identical to the volume setting in dBs (e.g. the 12C-bus data byte +10 sets the new volume value to +10 dB).

Balance can be realized by independent control of the left and right channel volume settings. Contour is adjustable between 0 and +18 dB with 1 dB resolution. This function is linked to the volume setting by means of microcontroller software.

Bass is adjustable between +15 and -12 dB with 1 dB resolution and treble is adjustable between +12 dB with 1 dB resolution.

For the purpose of a simple control software in the microcontroller, the decimal number that is sent as an I²C-bus data byte for contour, bass or treble is identical to the new contour, bass or treble setting in dBs (e.g. the I²C-bus data byte +8 sets the new value to +8 dB).

Extra bass boost is provided up to 20 dB with 2 dB resolution. The implemented coefficient set serves merely as an example on how to use this filter.

The beeper provides tones in a range from approximately 400 Hz to 30 kHz. The frequency can be selected via the I²C-bus. The beeper output signal is added to the loudspeaker and headphone channel signals. The beeper

volume is adjustable with respect to full scale between 0 and -93 dB with 3 dB resolution. The beeper is not effected by mute.

Soft mute provides a mute ability in addition to volume control with a well defined time (32 ms) after which the soft mute is completed. A smooth fading is achieved by a cosine masking.

6.2.5 HEADPHONE (AUXILIARY) CHANNEL

The matrix provides the following functions; forced mono, stereo, channel swap, channel 1 and channel 2 (or C and S in Dolby Surround Pro Logic mode).

Volume is controlled individually for each channel in a range from +24 to -83 dB with 1 dB resolution. There is also a mute position.

For the purpose of a simple control software in the microcontroller, the decimal number that is sent as an I²C-bus data byte for volume control is identical to the volume setting in dB (e.g. the 12C-bus data byte +10 sets the new volume value to +10 dB).

Balance can be realized by independent control of the left and right channel volume settings.

Bass is adjustable between +15 and -12 dB with 1 dB resolution and treble is adjustable between +12 dB with 1 dB resolution.

For the purpose of a simple control software in the microcontroller, the decimal number that is sent as an I²C-bus data byte for bass or treble is identical to the new bass or treble setting in dB (e.g. the 12C-bus data byte +8 sets the new value to +8 dB).

The beeper provides tones in a range from approximately 400 Hz to 30 kHz. The frequency can be selected via the I²C-bus. The beeper output signal is added to the loudspeaker and headphone channel signals. The beeper volume is adjustable with respect to full scale between 0 and -93 dB with 3 dB resolution. The beeper is not effected by mute.

Soft mute provides a mute ability in addition to volume control with a well defined time (32 ms) after which the soft mute is completed. A smooth fading is achieved by a cosine masking.

6.2.6 FEATURE INTERFACE

The feature interface comprises two I²S-bus input/output ports and a system clock output. Each I²S-bus port is equipped with level adjust facilities that can change the signal level in a range of ±15 dB with 1 dB resolution.

Outputs can be disabled to improve EMC performance. The I²S-bus output matrix provides the following functions; forced mono, stereo, channel swap, channel 1 and channel 2.

One example of how the feature interface can be used in a TV set is to connect an external Dolby Surround Pro Logic DSP, such as the SAA7710, to the I²S-bus ports. Outputs must be enabled and a suitable master clock signal for the DSP can be taken from pin SYSCLK.

A stereo signal from any source will be output on one of the I²S-bus serial data outputs and the four processed signal channels will be entered at both I²S-bus serial data inputs. Left and right could then be output to the power amplifiers via the Main channel, centre and surround via the Auxiliary channel.

6.2.7 CHANNEL FROM THE AUDIO ADC

The signal level at the output of the ADC can be adjusted in a range of ±15 dB with 1 dB resolution. The audio ADC itself is scaled to a gain of -6 dB.

6.2.8 CHANNEL TO THE ANALOG CROSSBAR PATH

Level adjust with control positions 0 dB, +3 dB, +6 dB and +9 dB.

6.2.9 DIGITAL CROSSBAR SWITCH (See Fig.6)

Input channels to the crossbar switch are from the audio ADC, I²S1, I²S2, FM path and from the loudspeaker channel path after matrix and AVL.

Output channels comprise loudspeaker, headphone, I²S1, I²S2 and the audio DACs for line output and SCART.

The I²S1 and I²S2 outputs also provide digital outputs from the loudspeaker and headphone channels, but without the beeper signals.

6.2.10 GENERAL

There are a number of functions that can provide signal gain, e.g. volume, bass and treble control. Great care has to be taken when using gain with large input signals in order not to exceed the maximum possible signal swing, which would cause severe signal distortion. The nominal signal level of the various signal sources to the digital crossbar switch should be 15 dB below digital full scale (15 dB full scale). This means that a volume setting of, say, +15 dB would just produce a full scale output signal and not cause clipping, if the signal level is nominal.

Sending illegal data patterns via the I²C-bus will not cause any changes of the current setting for the volume, bass, treble, bass boost and level adjust functions.

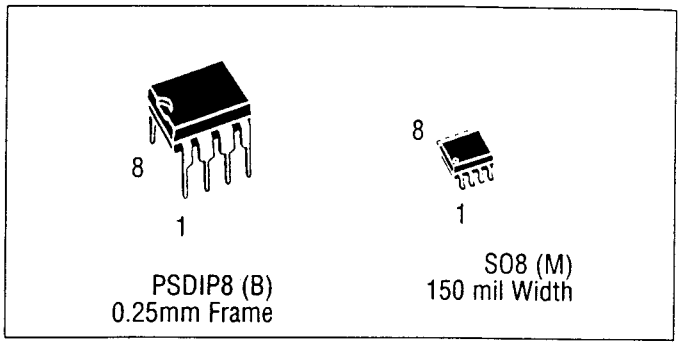
6.2.11 EXPERT MODE

The TDA9870A provides a special expert mode that gives direct write access to the internal Coefficient RAM (CRAM) of the DSP. It can be used to create user-defined characteristics, such as a tone control with different corner frequencies or special boost/cut characteristics to correct the low-frequency loudspeaker and/or cabinet frequency responses by means of the bass boost filter. However, this mode must be used with great care.

More information on the functions of this device, such as the number of coefficients per function, their default values, memory addresses, etc., can be made available

ST24C16, ST25C16, ST24W16, ST25W16
Serial 16 K (2K x 8) Eeprom

- **1 million erase/write cycles, with 40 years data retention**
- **Single supply voltage:**
  - 4.5V to 5.5V for ST24x16 versions
  - 2.5V to 5.5V for ST25x16 versions
- **Hardware write control versions:**
  ST24W16 and ST25W16
- **Two wire serial interface, fully I2C Bus compatible**
- **Byte and Multibyte write** (up to 8 bytes) for the ST24C16
- **Page write** (up to 16 bytes)
- **Byte, random and sequential read modes**
- **Self timed programming cycle**
- **Automatic address incrementing**
- **Enhanced ESD/Latch up performances**



DESCRIPTION

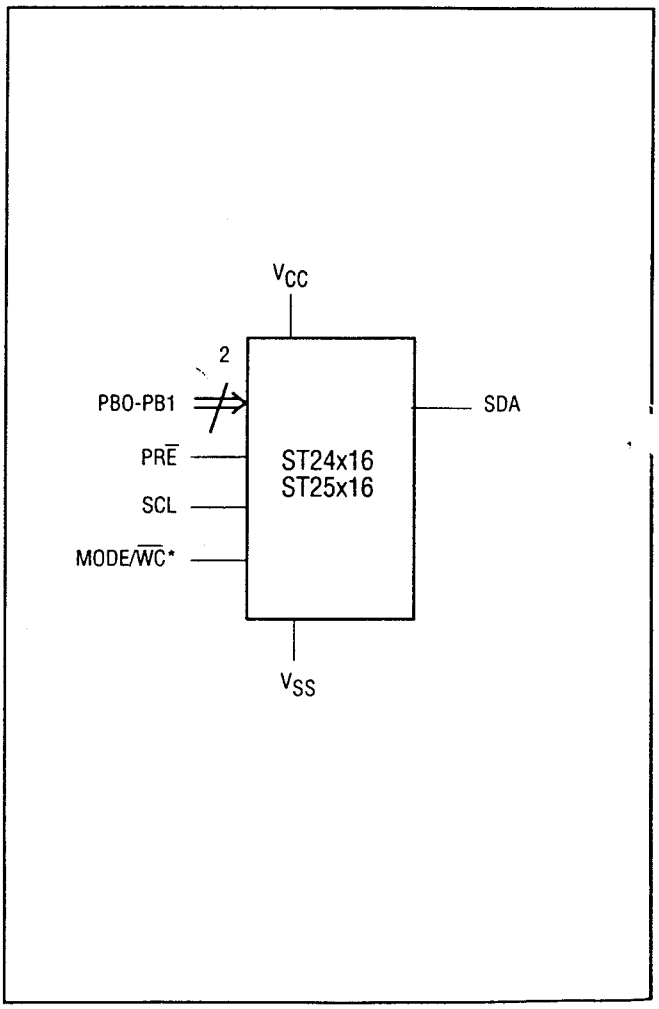
This specification covers a range of 16K bits I2C bus EEPROM products, the ST24/25C16 and the ST24/25W16. In the text, products are referred to as ST24/25x16 where "X" is: "C" for Standard version and "W" for hardware Write Control version.

The ST24/25x16 are 16K bit electrically erasable programmable memories (EEPROM), organized as 8 blocks of 256 x 8 bits. These are manufactured in SGS-Thomson's Hi-Endurance Advanced CMOS technology which guarantees an endurance of one million erase/write cycles with a data retention of 40 years. The ST25x16 operates with a power supply value as low as 2.5V. Both Plastic Dual-in-Line and Plastic Small Outline packages are Available.

Table 1. Signal Names

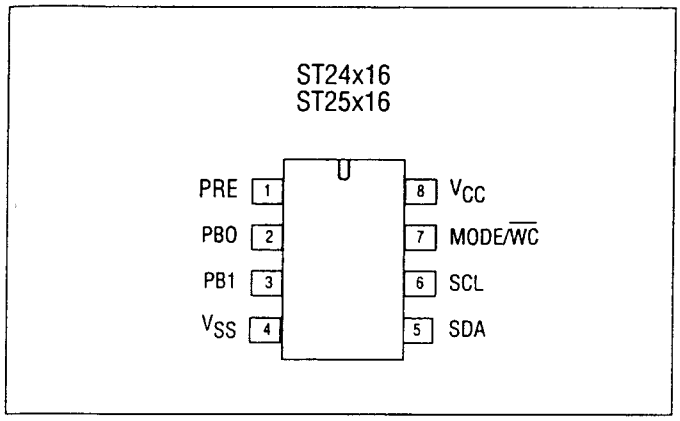
PRE	Write Protect Enable
PB0, PB1	Protect Block Select
SDA	Serial Data Address Input/Output
SCL	Serial Clock
MODE	Multybyte/Page Write Mode (C version)
$\overline{WC}$	Write Control (W version)
Vcc	Supply Voltage
Vss	Ground

Figure 1. Logic Diagram



Note: $\overline{WC}$ signal is only available for ST24/25W16 products

DIP Pin Connections



SO8 Pin Connections

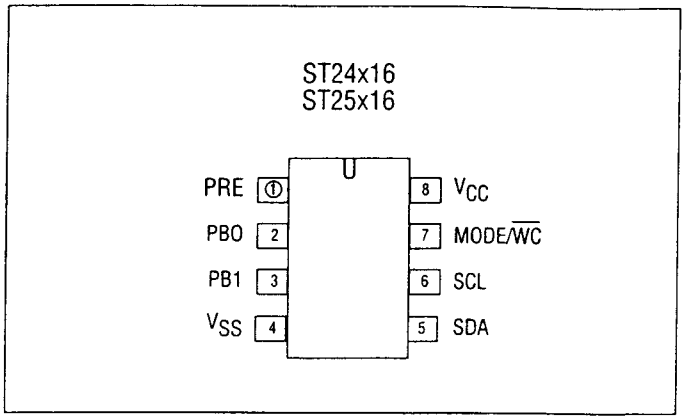


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature			-40 to 125	°C
T_{STG}	Storage Temperature			-65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8)	40 sec	215	°C
		(PSDIP8)	10 sec	260	°C
V_{IO}	Input or Output Voltage			-0.6 to 6.5	V
V_{CC}	Supply Voltage			-0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body Model) (2)			4000	V
	Electrostatic Discharge Voltage (Machine Model) (3)			500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. 100pF through 1500Ω; MIL-STD-883C, 3015.7
3. 200pF through 0Ω; EIAJ IC-121 (condition C)

DESCRIPTION

The memories are compatible with the I2C standard two wire serial interface which uses a bi-directional data bus and serial clock. The memories carry a built-in 4 bit, unique device identification code (1010) corresponding to the I2C bus definition. The memories behave as slave devices in the I2C protocol with all memory with all memory operations synchronized by the serial clock. Read and write operations are initiated by a START condition generated by the bus master. The START condition is followed by a stream of 4 bits (identification code 1010), 3 block select bits, plus one read/write bit and terminated by an acknowledge bit. When writing data to the memory it responds to the 8 bits received by asserting an acknowledge bit during the 9th bit time. When data is read by the bus master, it acknowledges the receipt of the data bytes in the same way. Data transfers are terminated with a STOP condition .

TDA8351
DC-coupled vertical deflection circuit

FEATURES

- Few external components
- Highly efficient fully DC-coupled vertical output bridge circuit
- Vertical flyback switch
- Guard circuit
- Protection against:
  - short - circuit of the output pins (7 and 4)
  - short - circuit of the output pins to Vp
- Temperature (thermal) protection
- High EMC immunity because of common mode inputs
- A quard signal in zoom mode.

GENERAL DESCRIPTION

The TDA8351 is a power circuit for use in 90° and 100° colour deflection systems for field frequencies of 50 to 120 Hz. The circuit provides a DC driven vertical deflection output circuit, operating as a highly efficient class G system.

QUICK REFERENCE DATA

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC supply						
V_P	supply voltage		9	-	25	V
I_q	quiescent supply current		-	30	-	mA
Vertical circuit						
$I_{O(p-p)}$	output current (peak-to-peak value)		-	-	3	A
$I_{diff(p-p)}$	differential input current (peak-to-peak value)		-	600	-	µA
$V_{diff(p-p)}$	differential input voltage (peak-to-peak value)		-	1.5	1.8	V
Flyback switch						
I_M	peak output current		-	-	±1.5	A
V_{FB}	flyback supply voltage	 note 1	- -	- -	50 60	V V
Thermal data (in accordance with IEC 747-1)						
T_{stg}	storage temperature		-55	-	+150	°C
T_{amb}	operating ambient temperature		-25	-	+75	°C
T_{vj}	virtual junction temperature		-	-	150	°C

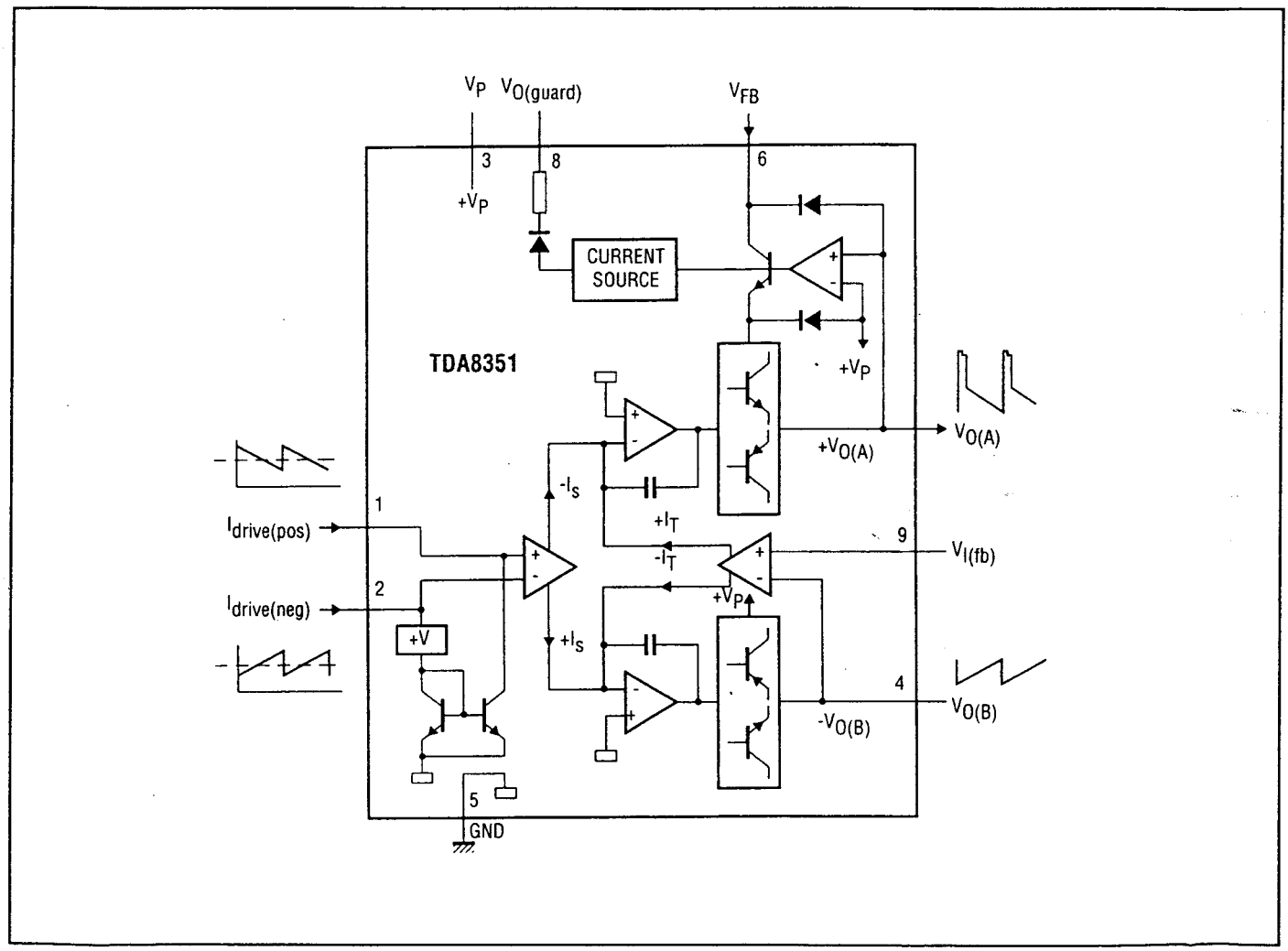
Note:

1- A flyback supply voltage of >50 V up to 60 V is allowed in application. A 220 nF capacitor in series with a 22Ω resistor (dependent on I_o and the inductance of the coil) has to be connected between pin 7 and ground. The decoupling capacitor of V_{FB} has to be connected between pin 6 and pin 3. This supply voltage line must have a resistance of 33 Ω (see application circuit Fig.G).

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8351	SIL9P	plastic single-in-line power package; 9 leads	SOT131-2

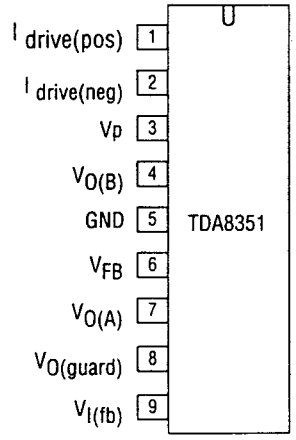
Block Diagram



PINNING

SYMBOL	PIN	DESCRIPTION
$I_{drive(pos)}$	1	input power-stage (positive); includes $I_{I(sb)}$ signal bias
$I_{drive(neg)}$	2	input power-stage (negative); includes $I_{I(sb)}$ signal bias
V_P	3	operating supply voltage
$V_{O(B)}$	4	output voltage B
GND	5	ground
V_{FB}	6	input flyback supply voltage
$V_{O(A)}$	7	output voltage A
$V_{O(guard)}$	8	guardoutput voltage
$V_{I(fb)}$	9	input feedback voltage

Pin Configuration



Metal block connected to substrate pin 5.
Metal on back

FUNCTIONAL DESCRIPTION

The vertical driver circuit is a bridge configuration. The deflection coil is connected between the output amplifiers, which are driven in phase opposition. An external resistor (RM) connected in series with the deflection coil provides internal feedback information. The differential input circuit is voltage driven. The input circuit has been adapted to enable it to be used with the TDA9150A, TDA9151B, TDA9160A, TDA9162, TDA8366 and TDA8376 which deliver symmetrical current signals. An external resistor (RCON) connected between the differential input determines the output current through the deflection coil. The relationship between the differential input current and the output current is defined by:

$I_{diff} \times R_{CON} = I_{coil} \times R_M$. The output current is adjustable from 0.5 A (p-p) to 3 A (p-p) by varying RM. The maximum input differential voltage is 1.8 V. In the application it is recommended that V_{diff} = 1.5 V (typ), This is recommended because of the spread of input current and the spread in the value of R_{CON}

The flyback voltage is determined by an additional supply voltage V_{FB}. The principle of operating with two supply voltages (class G) makes it possible to fix the supply voltage Vp optimum for the scan voltage and the second supply voltage V_{FB} optimum for the flyback voltage. Using this method, very high efficiency is achieved.

The supply voltage V_{FB} is almost totally available as flyback voltage across the coil, this being possible due to the absence of a decoupling capacitor (not necessary, due to the bridge configuration). The output circuit is fully protected against the following:

- thermal protection
- short-circuit protection of the output pins (pins 4 and 7)
- short-circuit of the output pins to Vp.

A guard circuit $V_{O(guard)}$ is provided. The guard circuit is activated at the following conditions:

- during flyback
- during short-circuit of the coil and during short-circuit of the output pins (pins 4 and 7) to Vp or ground
- during open loop
- when the thermal protection is activated.

This signal can be used for blanking the picture tube screen.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEJ 134)

Symbol	Parameter	Conditions	Min.	Max.	Unit
DC supply					
V_P	supply voltage	non-operating	-	40	V
			-	25	V
V_{FB}	flyback supply voltage		-	50	V
		note 1	-	60	V
Vertical circuit					
$I_{O(p-p)}$	output current (peak-to-peak value)	note 2	-	3	A
$V_{O(A)}$	output voltage (pin 7)		-	52	V
		note 1	-	62	V
Flyback switch					
I_M	peak output current		-	±1.5	A
Thermal data (in accordance with IEC 747-1)					
T_{stg}	storage temperature		-55	+150	°C
T_{amb}	operating ambient temperature		-25	+75	°C
T_{vj}	virtual junction temperature		-	150	°C
$R_{th\ vj-c}$	resistance v_j-case		-	4	K/W
$R_{th\ vj-a}$	resistance v_j-ambient in free air		-	40	K/W
Tsc	short-circuiting time	note 3	-	1	hr

Notes:

1. A flyback supply voltage of >50 V up to 60 V is allowed in application. A 220 nF capacitor in series with a 22Ω resistor (dependent on I_o and the inductance of the coil) has to be connected between pin 7 and ground. The decoupling capacitor of V_{FB} has to be connected between pin 6 and pin 3. This supply voltage line must have a resistance of 33 Ω (see application circuit Fig.6).
2. I_o maximum determined by current protection.
3. Up to Vp = 18V.

TDA8356
DC-coupled vertical deflection circuit

FEATURES

- Few external components
- Highly efficient fully DC-coupled vertical output bridge circuit
- Vertical flyback switch
- Guard circuit
- Protection against:
  - short - circuit of the output pins (7 and 4)
  - short - circuit of the output pins to Vp
- Temperature (thermal) protection
- High EMC immunity because of common mode inputs
- A quard signal in zoom mode.

GENERAL DESCRIPTION

The TDA8356 is a power circuit for use in 90° and 100° colour deflection systems for field frequencies of 50 to 120 Hz. The circuit provides a DC driven vertical deflection output circuit, operating as a highly efficient class G system.

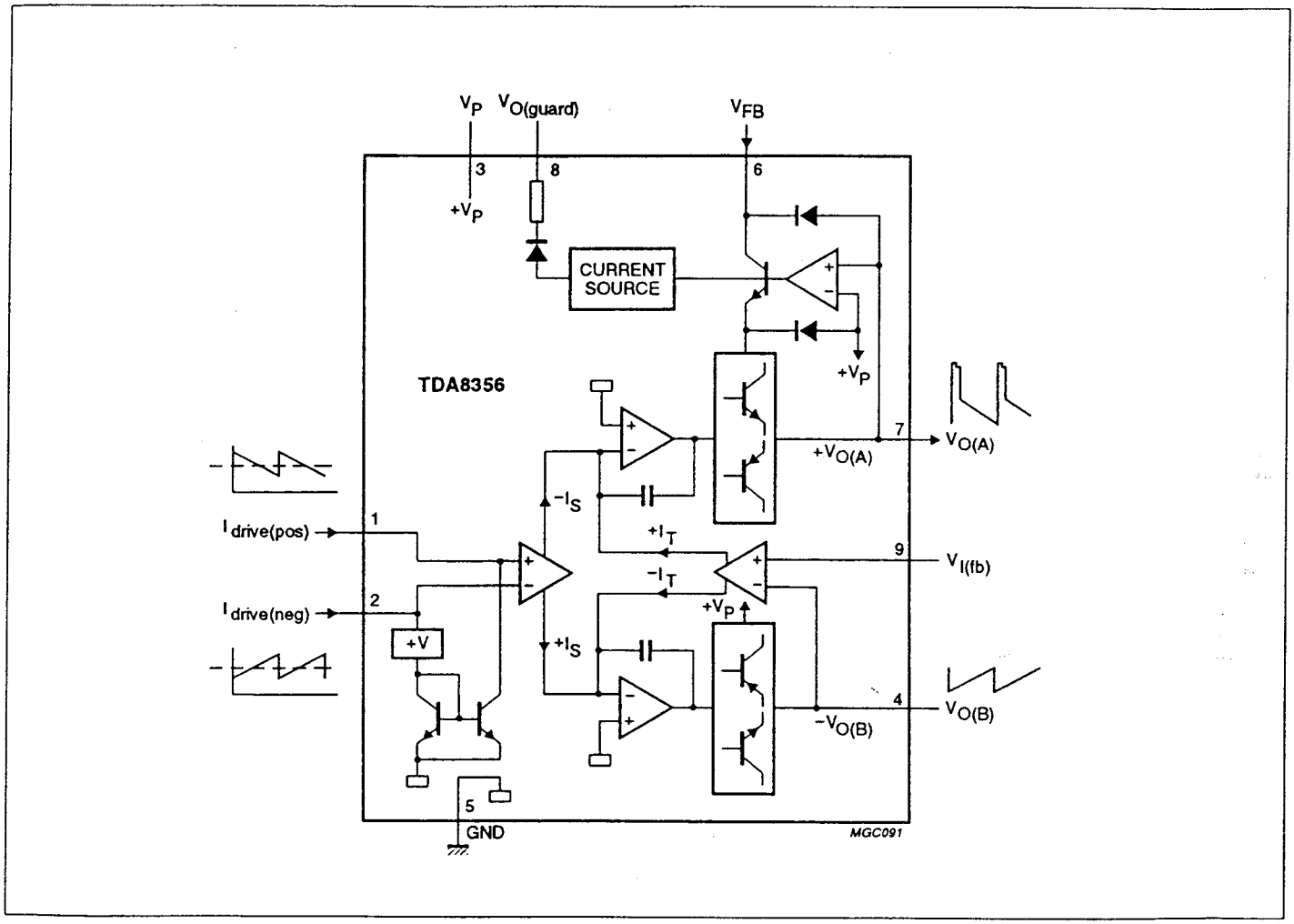
QUICK REFERENCE DATA

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC supply						
V_P	supply voltage		9	-	25	V
I_q	quiescent supply current		-	30	-	mA
Vertical circuit						
$I_{O(p-p)}$	output current (peak-to-peak value)		-	-	2	A
$I_{diff(p-p)}$	differential input current (peak-to-peak value)		-	600	-	µA
$V_{diff(p-p)}$	differential input voltage (peak-to-peak value)		-	1.5	1.8	V
Flyback switch						
I_M	peak output current		-	-	±1.5	A
V_{FB}	flyback supply voltage		-	-	50	V
Thermal data (in accordance with IEC 747-1)						
T_{stg}	storage temperature		-55	-	+150	°C
T_{amb}	operating ambient temperature		-25	-	+75	°C
T_{vj}	virtual junction temperature		-	-	150	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8356	SIL9P	plastic single-in-line power package; 9 leads	SOT131-2

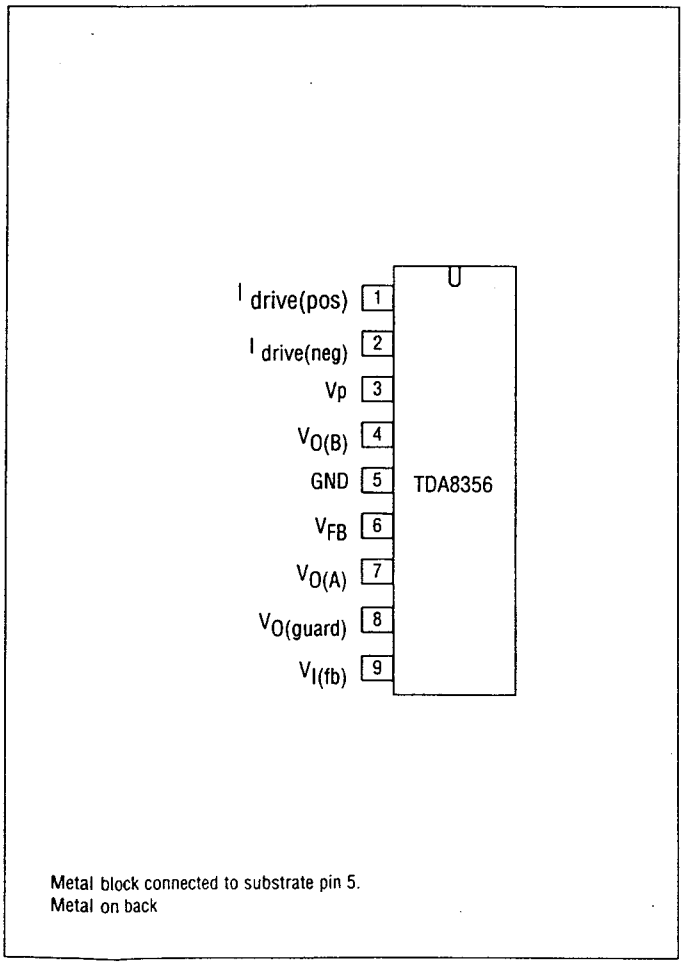
Block Diagram



PINNING

SYMBOL	PIN	DESCRIPTION
$I_{drive(pos)}$	1	input power-stage (positive); includes $I_{I(sb)}$ signal bias
$I_{drive(neg)}$	2	input power-stage (negative); includes $I_{I(sb)}$ signal bias
Vp	3	operating supply voltage
$V_{O(B)}$	4	output voltage B
GND	5	ground
V_{FB}	6	input flyback supply voltage
$V_{O(A)}$	7	output voltage A
$V_{O(guard)}$	8	guard output voltage
$V_{I(fb)}$	9	input feedback voltage

Pin Configuration



Metal block connected to substrate pin 5.
Metal on back

FUNCTIONAL DESCRIPTION

The vertical driver circuit is a bridge configuration. The deflection coil is connected between the output amplifiers, which are driven in phase opposition. An external resistor (R_M) connected in series with the deflection coil provides internal feedback information. The differential input circuit is voltage driven. The input circuit has been adapted to enable it to be used with the TDA9150, TDA9151B, TDA9160A, TDA9162, TDA8366 and TDA8376 which deliver symmetrical current signals. An external resistor (R_{CON}) connected between the differential input determines the output current through the deflection coil.

The relationship between the differential input current and the output current is defined by: $I_{diff} \times R_{CON} = I_{coil} \times R_M$. The output current is adjustable from 0.5 A (p-p) to 2 A (p-p) by varying R_M. The maximum input differential voltage is 1.8 V. In the application it is recommended that V_{diff} = 1.5 V (typ). This is recommended because of the spread of input current and the spread in the value of R_{CON}.

The flyback voltage is determined by an additional supply voltage V_{FB}. The principle of operating with two supply voltages (class G) makes it possible to fix the supply voltage Vp optimum for the scan voltage and the second supply voltage V_{FB} optimum for the flyback voltage. Using this method, very high efficiency is achieved. The supply voltage V_{FB} is almost totally available as flyback voltage across the coil, this being possible due to the absence of a decoupling capacitor (not necessary, due to the bridge configuration). The output circuit is fully protected against the following:

- thermal protection
- short-circuit protection of the output pins (pins 4 and 7)
- short-circuit of the output pins to Vp.

A guard circuit $V_{O(guard)}$ is provided. The guard circuit is activated at the following conditions:

- during flyback
- during short-circuit of the coil and during short-circuit of the output pins (pins 4 and 7) to Vp or ground
- during open loop
- when the thermal protection is activated.

This signal can be used for blanking the picture tube Screen.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEJ 134)

Symbol	Parameter	Conditions	Min.	Max.	Unit
DC supply					
V_P	supply voltage	non-operating	-	40	V
			-	25	V
V_{FB}	flyback supply voltage		-	50	V
Vertical circuit					
$I_{O(p-p)}$	output current (peak-to-peak value)	note 1	-	2	A
$V_{O(A)}$	output voltage (pin 7)		-	52	V
Flyback switch					
I_M	peak output current		-	±1.5	A
Thermal data (in accordance with IEC 747-1)					
T_{stg}	storage temperature		-55	+150	°C
T_{amb}	operating ambient temperature		-25	+75	°C
T_{vj}	virtual junction temperature		-	150	°C
$R_{th\ vj\text{-}c}$	resistance v_j-case		-	4	K/W
$R_{th\ vj\text{-}a}$	resistance v_j-ambient in free air		-	40	K/W
Tsc	short-circuiting time	note 2	-	1	hr

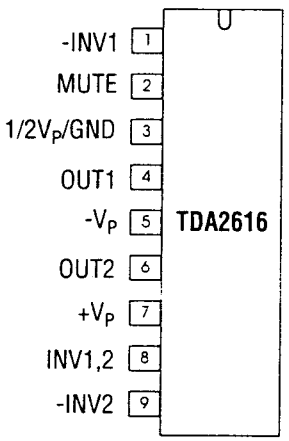
Notes

1. I_O maximum determined by current protection.
2. Up to V_p = 18 V.

TDA2616
2x12W Hi-Fi Audio Power Amplifiers with Mute

GENERAL DESCRIPTION
The TDA2616 is a dual power amplifiers. It has been especially designed for mains fed applications such as stereo radio and stereo TV.

FEATURES
- Requires very few external components
- No switch-on/switch-off clicks
- Input mute during switch-on and switch-off
- Low offset voltage between output and ground
- Excellent gain balance of both amplifiers
- Hi-Fi accordance with IEC 268 and DIN 45500
- Short-circuit proof and thermal protected
- Mute possibility.



Pin Configuration

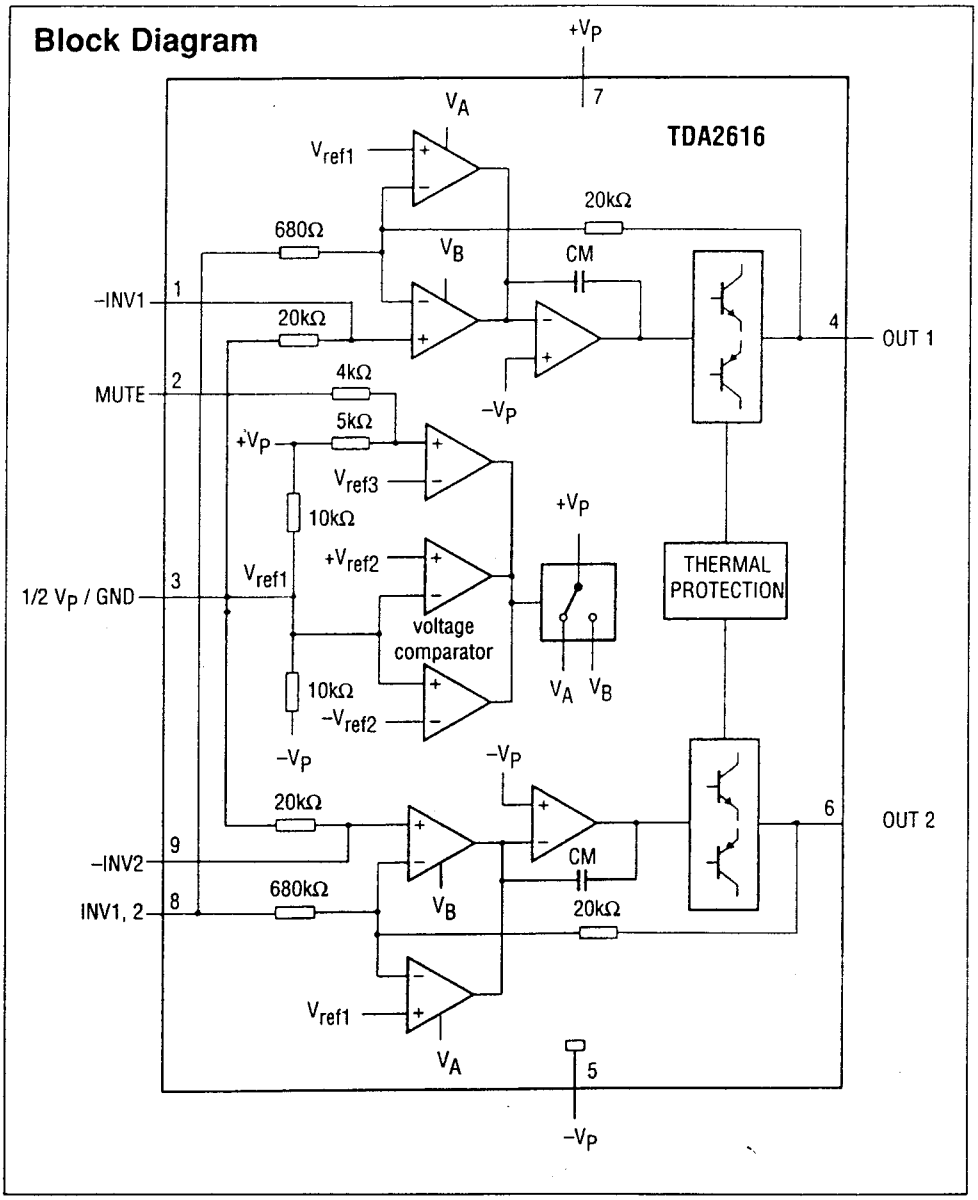
PINNING

Pin	Symbol	Function
1	-INV1	non-inverting input 1
2	MUTE	mute input
3	1/2V_P/GND	1/2 supply voltage or ground
4	OUT1	output 1
5	-V_P	supply voltage (negative)
6	OUT2	output 2
7	+V_P	supply voltage (positive)
8	INV1,2	inverting inputs 1,2
9	-INV2	non-inverting input 2

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	Min.	Typ.	Max.	Unit
$\pm V_P$	supply voltage range		7.5	-	21	V
P_O	output power	V_P = ±16V; THD = 0.5%	-	12	-	W
G_V	internal voltage gain		-	30	-	dB
$\lvert G_V \rvert$	channel unbalance		-	0.2	-	dB
α	channel separation		-	70	-	dB
SVRR	supply voltage ripple rejection		-	60	-	dB
V_{no}	noise output voltage		-	70	-	µV

Block Diagram



LIMITING VALUES

In accordance with the Absolute maximum System (IEC 134)

Symbol	Parameter	Conditions	Min.	Max.	Unit
$\pm V_P$	supply voltage		-	21	V
I_{OSM}	non-repetitive peak output current		–	4	A
P_{tot}	total power dissipation		–	25	W
T_{stg}	storage temperature range		–55	+150	°C
T_{XTAL}	crystal temperature		–	+150	°C
T_{amb}	ambient operating temperature range		–25	150	°C
Tsc	short circuit time	short-circuit to ground; note 1	–	1	h

Note to the limiting values

1. For asymmetrical power supplies (with the load short-circued), the maximum unloaded supply voltage is limited to V_P = 28 V and with an internal supply resistance of $R_S \geq 4\Omega$, the maximum unloaded supply voltage is limited to 32 V (with the load short-circuited). For symmetrical power supplies the circuit is short-circuit-proof up to V_P=±21V.

TDA2615
2x6 W Hi-Fi Audio Power Amplifiers with Mute

FEATURES
- Requires very few external components
- No switch-on/switch-off clicks
- Input mute during switch-on and switch-off
- Low offset voltage between output and ground
- Excellent gain balance of both amplifiers
- Hi-Fi accordance with "IEC 268" and "DIN 45500"
- Short-circuit proof and thermal protected
- Mute possibility.

GENERAL DESCRIPTION
The TDA2615 is a dual power amplifier in a 9-lead plastic single-in-line (SIL9MPF) medium power package. It has been especially designed for mains fed applications such as stereo radio and stereo TV.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
±VP	supply voltage range		7.5	-	21	V
PO	output power	VS = ±12V; THD = 0.5%	-	6	-	W
GV	internal voltage gain		-	30	-	dB
|GV|	channel unbalance		-	0.2	-	dB
α	channel separation		-	70	-	dB
SVRR	supply voltage ripple rejection		-	60	-	dB
VNO	noise output voltage		-	70	-	μV

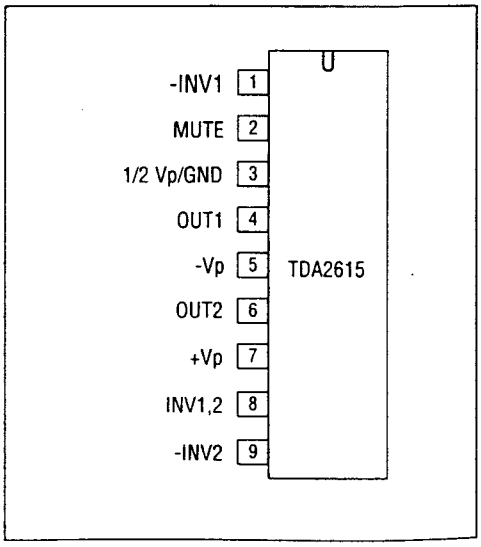
ORDERING INFORMATION

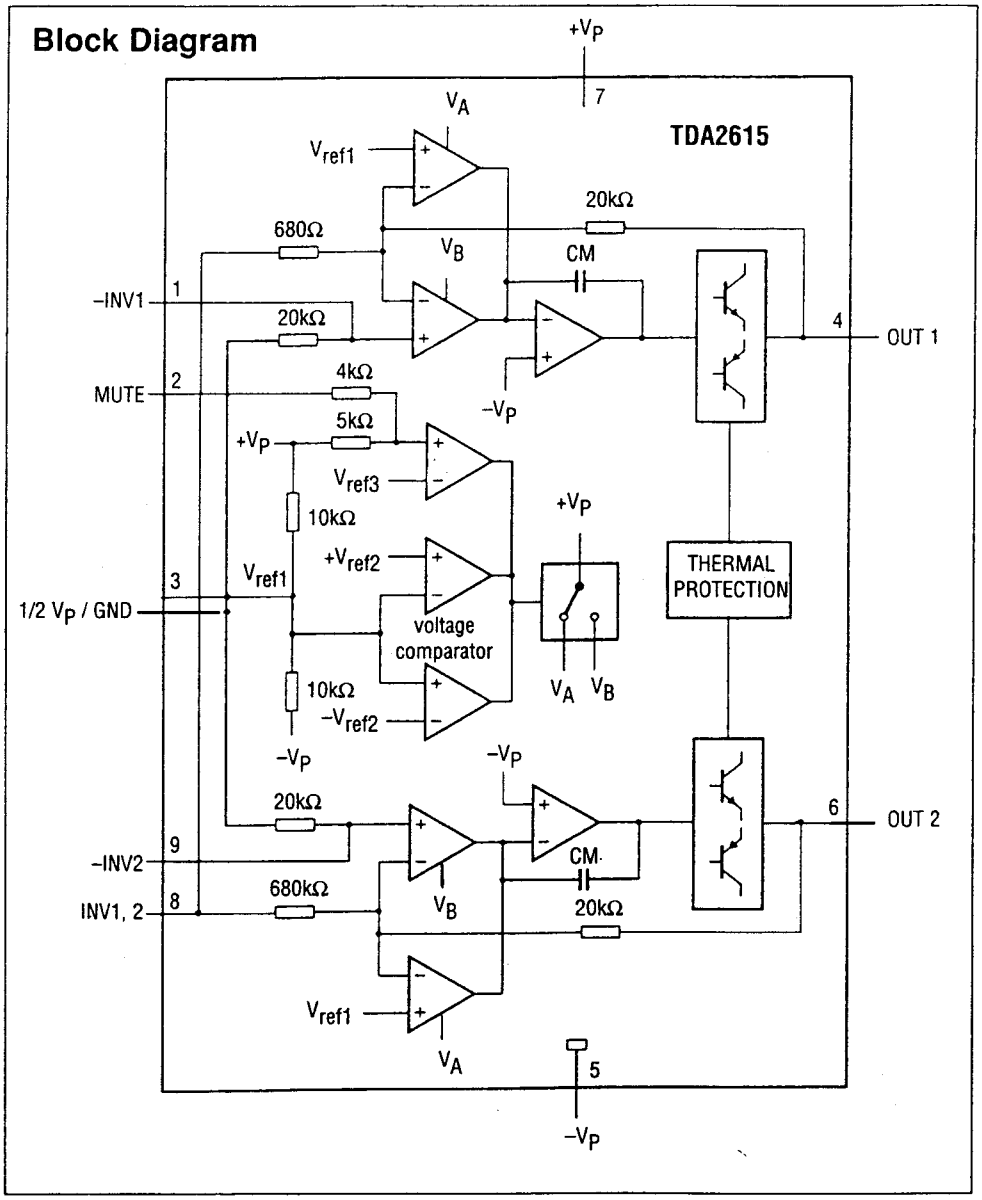
TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA2615	SIL9PPF	plastic single-in-line medium power package with fin ; 9 leads	SOT110-1

PINNING

SYMBOL	PIN	DESCRIPTION
-INV1	1	non-inverting input 1
MUTE	2	mute input
1/2 Vp/GND	3	1/2 supply voltage or ground
OUT 1	4	output 1
-Vp	5	supply voltage (negative)
OUT 2	6	output 2
+Vp	7	supply voltage (positive)
INV1, 2	8	inverting input 1 and 2
-INV2	9	non-inverting input 2

Pin Configuration





FUNCTIONAL DESCRIPTION

The TDA2615 is a hi-fi stereo amplifier designed for mains fed applications, such as stereo radio and TV. The circuit is optimally designed for symmetrical power supplies, but is also well-suited to asymmetrical power supply systems.

An output power of 2 x 6 W (THD = 0.5%) can be delivered into an 8 Ω load with asymmetrical power supply of ±12 V. The gain is internally fixed at 30 dB, thus offering a low gain spread and a very good gain balance between the two amplifiers (0.2 dB).

A special feature is the input mute circuit. This circuit disconnects the non-inverting inputs when the supply voltage drops below ±6 V, while the amplifier still retains its DC operating adjustment. The circuit features suppression of unwanted signals at the inputs, during switch-on and switch-off.

The mute circuit can also be activated via pin 2. When a current of 300 µA is present at pin 2, the circuit is in the mute condition.

The device is provided with two thermal protection circuits. One circuit measures the average temperature of the crystal and the other measures the momentary temperature of the power transistors. These control circuits attack at temperatures in excess of +150 °C, so a crystal operating temperature of max. +150 °C can be used without extra distortion. With the derating value of 6 K/W, the heatsink can be calculated as follows:

at R_L = 8 Ω and V_S = ±12 V. The measured maximum dissipation is 7.8 W.

With a maximum ambient temperature of +60 °C, the thermal resistance of the heatsink is:

$$R_{th} = \frac{150 - 60}{7.8} - 6 = 5.5 \text{ K/W}.$$

The internal metal block has the same potential as Pin 5.

CHARACTERISTICS

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Supply						
$\pm V_P$	supply voltage range		-	12	21	V
I_{ORM}	repetitive peak output current		2.2	-	-	A
Operating position; note 1						
$\pm V_P$	supply voltage range		7.5	12	21	V
$I_{q(tot)}$	total quiescent current	$R_L = \infty$	18	40	70	mA
P_o	output power	THD = 0.5%	5	6	-	W
		THD = 10%	6.5	8	-	W
THD	total harmonic distortion	Po = 4W	-	0.15	0.2	%
B	power bandwidth	THD = 0.5%; note 2	-	20 to 20000	-	Hz
G_V	voltage gain		29	30	31	dB
$\lvert G_V \rvert$	gain unbalance		-	0.2	1	dB
V_{no}	noise output voltage	note 3	-	70	140	µV
$\lvert Z_I \rvert$	input impedance		14	20	26	kΩ
SVRR	supply voltage ripple rejection	note 4	40	60	-	dB
α_{cs}	channel separation	Rs = 0	46	70	-	dB
I_{bias}	input bias current		-	0.3	-	µA
$\lvert \Delta V_{GND} \rvert$	DC output offset voltage		-	30	200	mV
$\lvert \Delta V_{4-6} \rvert$	DC output offset voltage	between two channels	-	4	150	mV
MUTE POSITION (AT $I_{MUTE} \geq 300\mu A$)						
V_o	output voltage	V_I = 600 mV	-	0.3	1.0	mV
Z_{2-7}	mute input impedance		-	9	-	kΩ
$I_{q(tot)}$	total quiescent current	$R_L = \infty$	18	40	70	mA
V_{no}	noise output voltage	note 3	-	70	140	µA
SVRR	supply voltage ripple rejection	note 4	40	55	-	dB
$\lvert \Delta V_{GND} \rvert$	DC output offset voltage		-	40	200	mV
$\lvert \Delta V_{off} \rvert$	offset voltage with respect to operating position		-	4	150	mV
I_2	current if pin 2 is connected to pin 5		-	-	6	mA
Mute position; note 5						
$\pm V_p$	supply voltage range		2	-	5.8	V
I_p	total quiescent current	$R_L = \infty$	9	30	40	mA
V_o	output voltage	V_I = 600 mV	-	0.3	1.0	mV
V_{no}	noise output voltage	note 3	-	70	140	µV
SVRR	supply voltage ripple rejection	note 4	40	55	-	dB
$\lvert \Delta V_{GND} \rvert$	DC output offset voltage		-	40	200	mV

TDA7056
3 W mono BTL audio output amplifier

FEATURES
- No external components
- No switch-on/off clicks
- Good overall stability
- Low power consumption
- Short circuit proof
- ESD protected on all pins.

GENERAL DESCRIPTION
The TDA8351 is a mono output amplifier contained in a 9 pin medium power package.
The device is designed for battery-fed portable mono recorders, radios and television.

QUICK REFERENCE DATA

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_P	supply voltage		3	11	18	V
P_O	output power in 16 Ω	V_P = 11V	2.5	3	-	W
G_v	internal voltage gain		39	40.5	42	dB
I_P	total quiescent current	V_P = 11V; R_L = ∞	-	5	7	mA
THD	total harmonic distortion	P_O = 0.5W	-	0.25	1	%

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA7056	9	SIL	plastic	SOT110[1]

Note
1. SOT110-1; 1996 August 21.

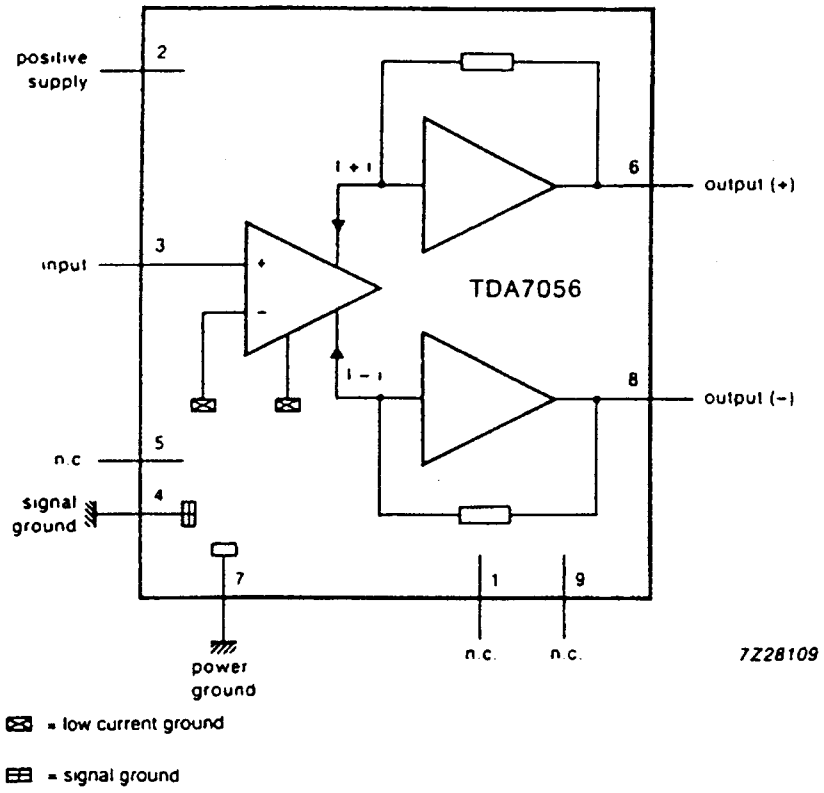
PINNING

PIN	DESCRIPTION
1	n.c
2	Vp
3	input (+)
4	signal ground
5	n.c.
6	output (+)
7	power ground
8	output (–)
9	n.c.

FUNCTIONAL DESCRIPTION
The TDA7056 is a mono output amplifier, designed for battery-fed portable radios and mains-fed equipment such as television. For space reasons there is a trend to decrease the number of external components. For portable applications there is also a trend to decrease the number of battery cells, but still a reasonable output power is required.

The TDA7056 fulfills both of these requirements. It needs no peripheral components, because it makes use of the Bridge-Tied-Load (BTL) principle. Consequently it has, at the same supply voltage, a higher output power compared to a conventional Single Ended output stage. It delivers an output power of 1 W into a loudspeaker load of 8 Ω with 6 V supply or 3 W into 16 Ω loudspeaker at 11 V without need of an external heatsink. The gain is internally fixed at 40 dB. Special attention is given to switch-on/off click suppression, and it has a good overall stability. The load can be short circuited at all input conditions.

Description of the DSP



CHARACTERISTICS

At Tamb = 25 °C; f = 1kHz; Vp = 11V; RL = 16Ω (see Fig. 2)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_P	operating supply voltage		3	11	18	V
I_{ORM}	repetitive peak output current		–	–	0.6	A
I_q	total quiescent current	note 1 $R_L = \infty$	–	5	7	mA
P_o	output power	THD = 10%	2.5	3	–	W
THD	total harmonic distortion	P_o = 0.5W	–	0.25	1	%
G_v	voltage gain		39	40.5	42	dB
V_{no}	noise output voltage	note 2	–	180	300	μV
V_{no}	noise output voltage	note3	–	60	–	μV
	frequency response		–	20 to 20.000	–	Hz
RR	ripple rejection	note 4	36	50	–	dB
ΔV	DC-output offset voltage	note 5	–	–	200	mV
Z_i	input impedance		–	100	–	kΩ
I_i	input bias current		–	100	300	nA

Notes to the characteristics

1. With a load connected to the outputs the quiescent current will increase, the maximum value of this increase being equal to the DC output offset voltage divided by R_L.
2. The noise output voltage (RMS value) is measured with R_S = 5 kΩ unweighted (20 Hz to 20 kHz).
3. The noise output voltage (RMS value) at f = 500 kHz is measured with Rs = 0 Ω and bandwidth = 5 kHz. With a practical load (R_L = 16Ω, L_L = 200 μH) the noise output current is only 50 nA.
4. The ripple rejection is measured with R_S = 0 Ω and f = 100 Hz to 10 kHz.
   The ripple voltage (200 mV) is applied to the positive supply rail.
5. R_S=5kΩ.

TDA7057AQ

2 x5 W stereo BTL Audio Output Amplifier with DC Volume Control

FEATURES

- DC volume control
- Few external components
- Mute mode
- Thermal protection
- Short-circuit proof
- No switch-on and switch-off clicks
- Good overall stability
- Low power consumption
- Low HF radiation
- ESD protected on all pins.

GENERAL DESCRIPTION

The TDA7057AQ is astereo BTL output amplifier with DC volume control. The device is designed for use in TV and monitors, but are also suitable for battery-fed portable recorders and radios.

Missing Current Limiter (MCL)

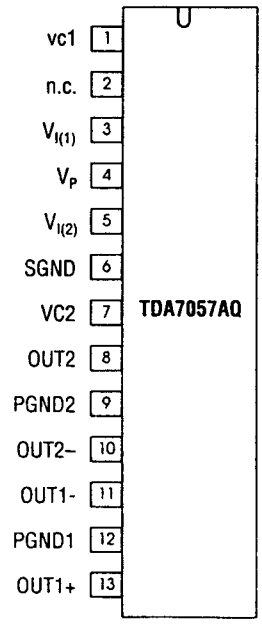
A MCL protection circuit is built-in. The MCL circuit is activated when the difference in current between the output terminal of each amplifier exceeds 100 mA (typical 300 mA). This level of 100 mA allows for headphone applications (single-ended).

QUICK REFERENCE DATA

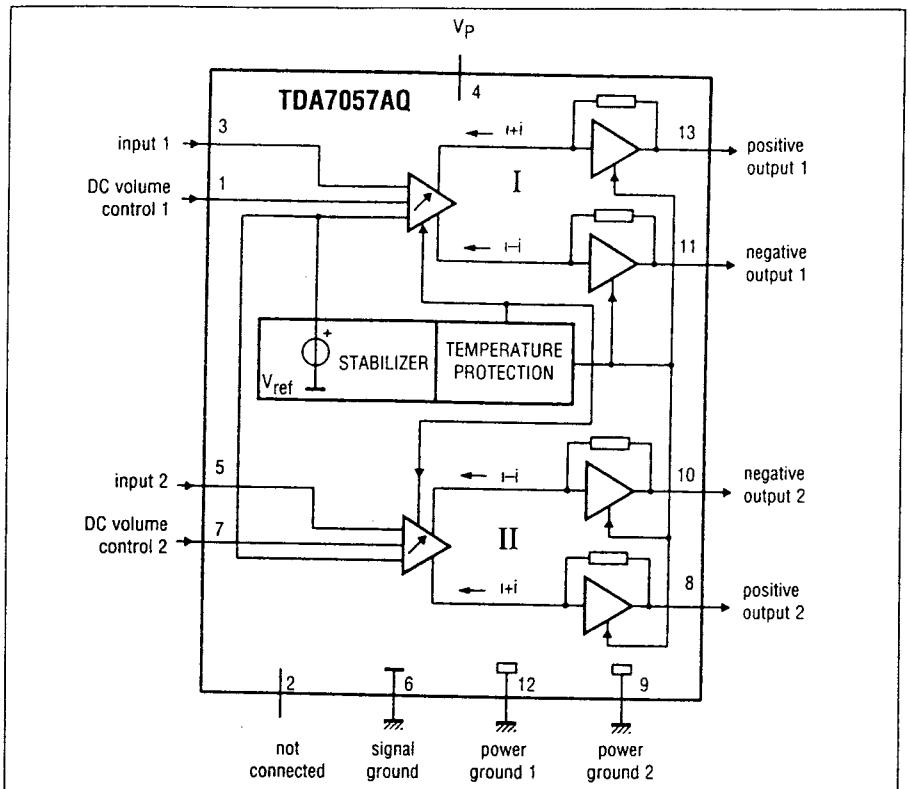
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage		4.5	–	18	V
P_{out}	output power	V_p = 12 V; R_L = 16 Ω	3.0	3.5	–	W
		V_p = 12 V; R_L = 8Ω	–	5.3	–	W
G_v	voltage gain		39.5	40.5	41.5	dB
G_C	gain control		68.0	73.5	–	dB
$I_{q(tot)}$	total quiescent current	V_p = 12 V; R_L = ∞	–	22	25	mA
THD	total harmonic current	P_{out}=0.5w w	–	0.3	1	%

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA7057AQ	DBS13P	Plastic DIL-bent-SIL power package; 13 leads (lead length 12 mm)	SOT141-6

SYMBOL	PIN	DESCRIPTION
VC1	1	DC volume contol 1
n.c.	2	not connected
$V_{I(1)}$	3	voltage input 1
V_P	4	positive supply voltage
$V_{I(2)}$	5	voltage input 2
SGND	6	signal ground
VC2	7	DC volume contol 2
OUT2+	8	positeve output 2
PGND2	9	power ground 2
OUT2-	10	negative output 2
OUT1-	11	negative output 1
PGND1	12	powwer ground 1
OUT1+	13	positive output 1



Pin Configuration



Block diagram

FUNCTIONAL DESCRIPTION

The TDA7057AQ is a stereo output amplifiers with two DC volume control stages. The device is designed for TV and monitors, but also suitable for battery-fed portable recorders and radios.

In conventional DC volume control circuits the control or input stage is AC coupled to the output stage via external capacitors to keep the offset voltage low.

In the TDA7057AQ the two DC volume control stages are integrated into the input stages so that no coupling capacitors are required and a low offset voltage is still maintained. The minimum supply voltage also remains low.

The BTL principle offers the following advantages:

- Lower peak value of the supply current
- The frequency of the ripple on the supply voltage is twice the signal frequency.

Consequently, a reduced power supply with smaller capacitors can be used which results in cost reductions.

For portable applications there is a trend to decrease the supply voltage, resulting in a reduction of output power at conventional output stages. Using the BTL principle increases the output power.

The maximum gain of the amplifier is fixed at 40.5 dB. The DC volume control stages have a logarithmic control characteristic. Therefore, the total gain can be controlled from +40.5 dB to -33 dB. If the DC volume control voltage falls below 0.4 V, the device will switch to the mute mode.

The amplifier is short-circuit protected to ground, Vp and across the load. A thermal protection circuit is also implemented. If the crystal temperature rises above 150 oC the gain will be reduced, thereby reducing the output power.

Special attention is given to switch-on and switch-off clicks, low HF radiation and a good overall stability.

TDA7050
Low voltage mono/stereo power amplifier

GENERAL DESCRIPTION
The TDA7050 is a low voltage audio amplifier for small radios with headphones (such as watch, pen and pocket radios) in mono (bridge-tied load) or stereo applications.

FEATURES
- Limited to battery supply application only (typ. 3 and 4 V)
- Operates with supply voltage down to 1.6 V
- No external components required
- Very low quiescent current
- Fixed integrated gain of 26 dB, floating differential input
- Flexibility in use - mono BTL as well as stereo
- Small dimension of encapsulation (see package design example)

QUICK REFERENCE DATA

Supply voltage range	Vp	1.6 to 6.0V	
Total quiescent current (at V_p = 3V)	Itot	typ.	3.2 mA
Bridge tied load application (BTL)			
Output power at RL = 32Ω			
V_p = 3V; d_{tot} = 10%	Po	TYP.	140 mW
D.C. output offset voltage between the outputs	ΔV	max	70 mV
noise output voltage (r.m.s. value)			
at f = 1 kHz; R_S = 5Ω	Vno(rms)	typ.	140μV
Stereo applications			
Output power at R_L = 32Ω			
d_{tot} =10%; V_p = 3V	Po	typ.	35 mW
d_{tot} =10%; V_p = 4.5V	Po	typ.	75mW
Channel separation at Rs = 0Ω; f = 1 kHz	α	typ.	40 dB
noise output voltage (r.m.s. value)			
at f = 1 kHz; R_S = 5Ω	Vno(rms)	typ.	100μV

PACKAGE OUTLINE
8 -lead DIL; plastic (SOT97); SOT97-1; 1996 July 23.

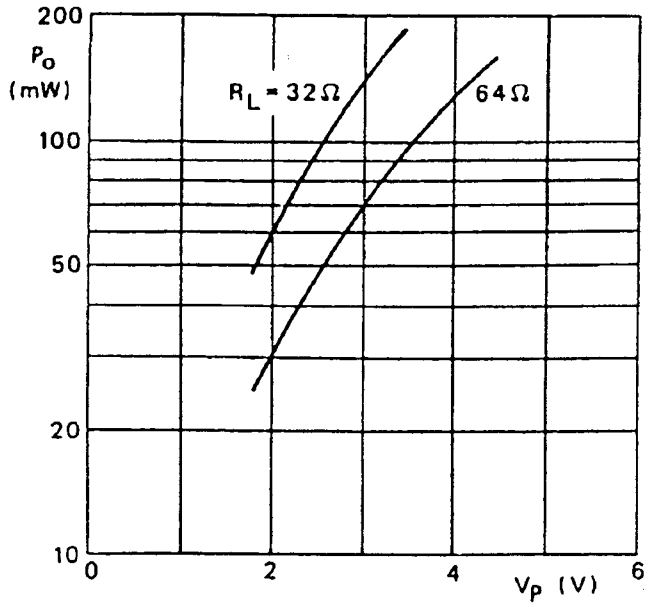


Fig. 2 Output power across the load impedance (R_L) as a function of supply voltage (V_P) in BTL application. Measurements were made at f = 1 kHz; d_{tot} = 10%; T_{amb} = 25 °C

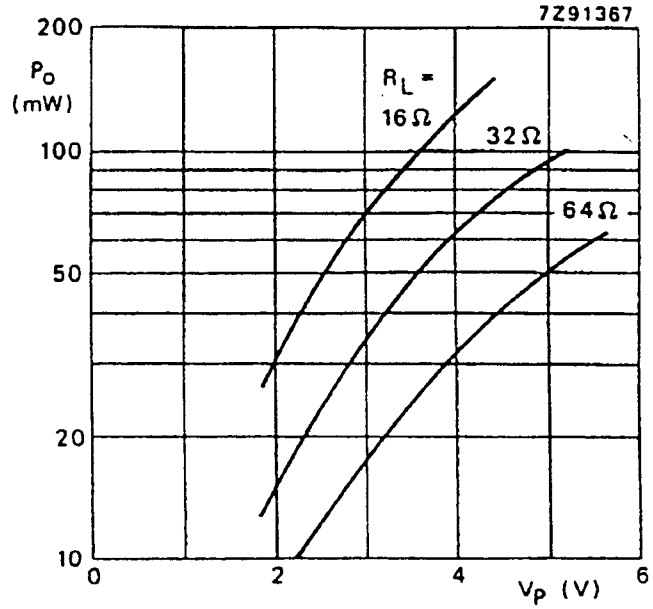


Fig. 3 Output power across the load impedance (R_L) as a function of supply voltage (V_P) in stereo application. Measurements were made at f = 1 kHz; d_{tot} = 10%; T_{amb} = 25 °C

CHARACTERISTICS

V_p = 3V; f = 1 kHz; R_L = 32 Ω; T_{amb} = 25 °C; unless otherwise specified

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	Vp	1.6	–	6.0	V
Total guiescent current	Itot	–	3.2.	4	mA
Bridge tied load application (BTL); see Fig.4					
Output power; note 1					
V_p = 3.0V; d_{tot} = 10%	P_o	–	140	–	mW
V_p = 4.5V; d_{tot} = 10% (R_L = 64Ω)	P_o	–	150	–	mW
Voltage gain	G_v	–	32	–	dB
Noise output voltage (r.m.s. value)					
R_S = 5Ω; f = 1 kHz;	$V_{no(rms)}$	–	140	–	μV
R_S = 0Ω; f = 500 kHz; B = 5 kHz	$V_{no(rms)}$	–	tbf	–	μV
D.C. output offset voltage (at R_S = 5Ω)	$\lvert\Delta V\rvert$	–	–	70	mV
input impedance (at Rs = ∞)	$\lvert Z_i\rvert$	–	–	–	MΩ
input bias current	I_i	–	40	–	nA
Stereo applications; see Fig 5					
Output power; note 1					
V_p = 3.0V; d_{tot} = 10%	P_o	–	35	–	mW
V_p = 4.5V; d_{tot} = 10%	P_o	–	75	–	mW
Voltage gain	G_v	24.5	26	27.5	dB
Noise output voltage (r.m.s. value)					
R_S = 5Ω; f = 1 kHz;	$V_{no(rms)}$	–	100	–	μV
R_S = 0Ω; f = 500 kHz; B = 5 kHz	$V_{no(rms)}$	–	tbf	–	μV
Channel separation					
Rs = 0Ω; f = 1 kHz	α	30	40	–	dB
input impedance (at Rs = ∞)	$\lvert Z_i\rvert$	2	–	–	MΩ
input bias current	I_i	–	20	–	nA

Note

1. Output power is measured directly at the output pins of the IC. It is shown as a function of the supply voltage in Fig. 2 (BTL application) and Fig. 3 (stereo application).

TDA6107Q
Triple video output amplifier

FEATURES

- Typical bandwidth of 5.5 MHz for an output signal of 60 V (peak-to-peak value)
- High slew rate of 900 V/μs
- No external components required
- Very simple application
- Single supply voltage of 200 V
- Internal reference voltage of 2.5 V
- Fixed gain of 50
- Black-Current Stabilization (BCS) circuit
- Thermal protection.

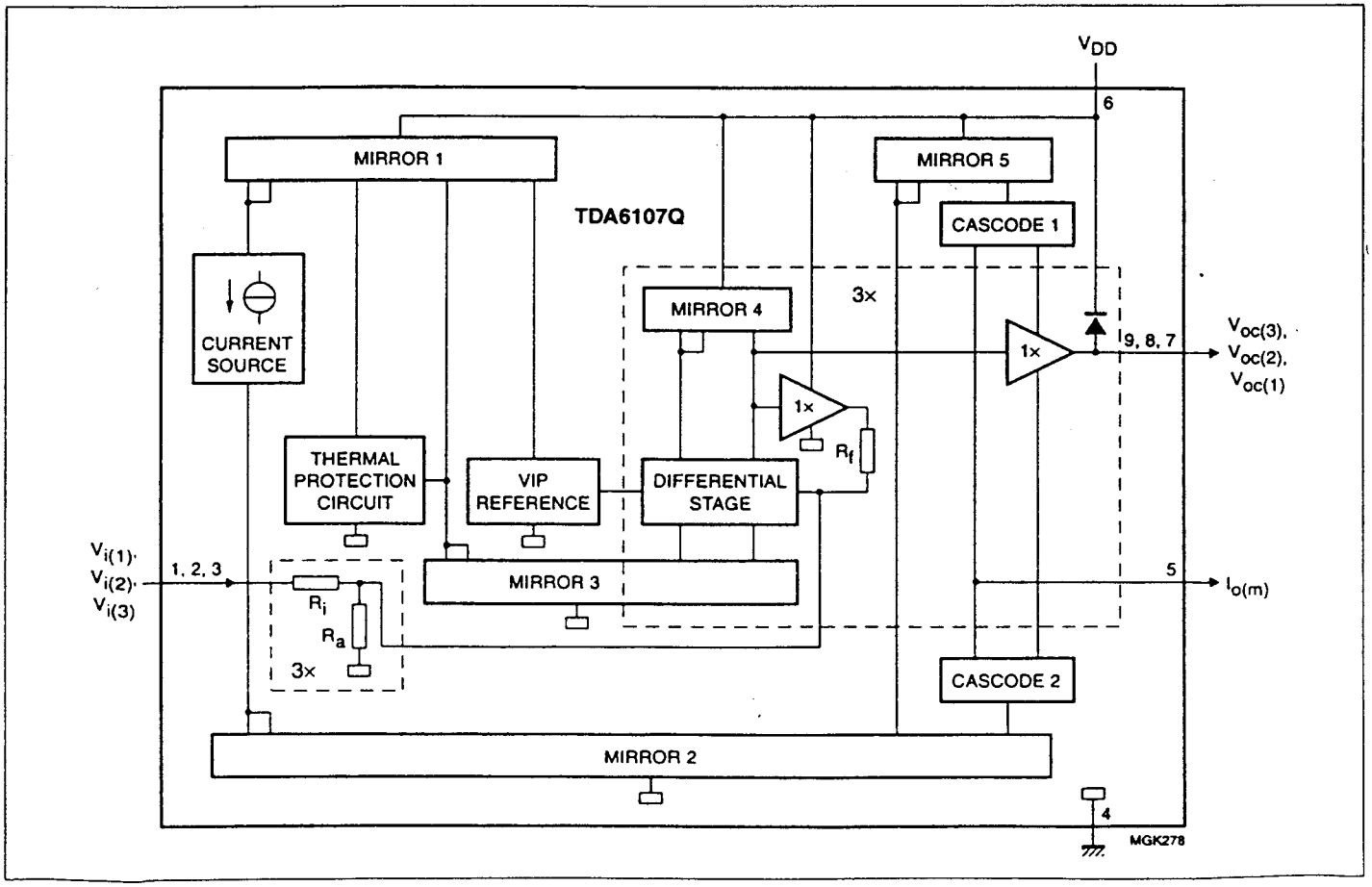
GENERAL DESCRIPTION

The TDA6107Q includes three video output amplifiers in one plastic DIL-bent-SIL 9-pin medium power (DBS9MPF) package (SOT111-1), using high-voltage DMOS technology, and is intended to drive the three cathodes of a colour CRT directly. To obtain maximum performance, the amplifier should be used with black -current control.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA6107Q	DBS9MPF	plastic DIL-bent-SIL medium power package with fin; 9 leads	SOT111-1

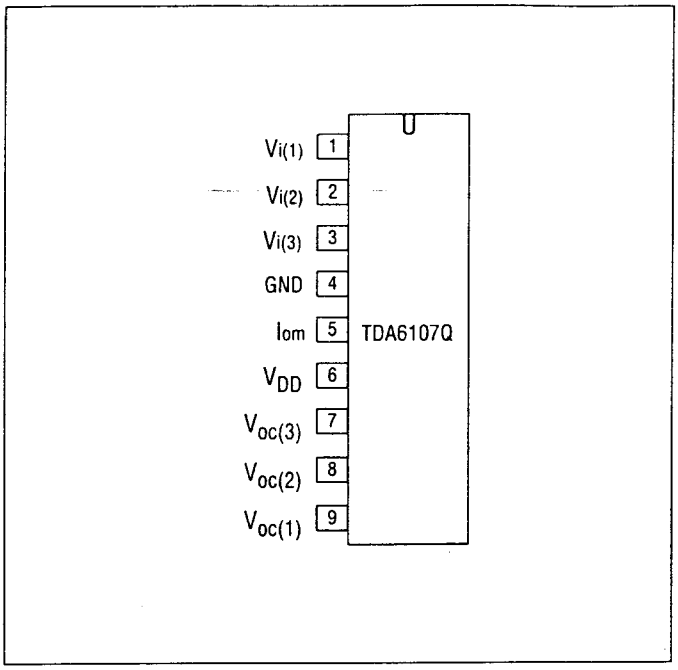
Block Diagram



PINNING

SYMBOL	PIN	DESCRIPTION
$V_{i(1)}$	1	inverting input 1
$V_{i(2)}$	2	inverting input 2
$V_{i(3)}$	3	inverting input 3
GND	4	ground (fin)
I_{om}	5	black current measurement output
V_{DD}	6	supply voltage
$V_{oc(3)}$	7	cathode output 3
$V_{oc(2)}$	8	cathode output 2
$V_{oc(1)}$	9	cathode output 1

Pin Configuration



LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); voltages measured with respect to pin 4 (ground); currents as specified in Fig. 1; unless otherwise specified.

No	Symbol	Parameter	Min.	Max.	Unit
101	V_{DD}	supply voltage	0	250	V
102	V_i	input voltage at pins 1 to 3	0	12	V
103	$V_{o(m)}$	measurement output voltage	0	6	V
104	$V_{o(c)}$	cathode output voltage	0	V_{DD}	V
107	T_{stg}	storage temperature	-55	+150	°C
108	T_j	junction temperature	-20	+150	°C
	Ves	electrostatic handling			
109		Human Body Model (HBM)	-	2000	V
110		Machine Model (MM)	-	300	V

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see "Handling MOS Devices").

QUALITY SPECIFICATION

Quality specification "SNW-FQ-611 part D" is applicable and can be found in the "Quality reference Handbook".

The handbook can be ordered using the code 9397 750 00192.

TCDT1100(G) Series
Optocoupler with Phototransistor Output

FEATURES

According to VDE 0884:

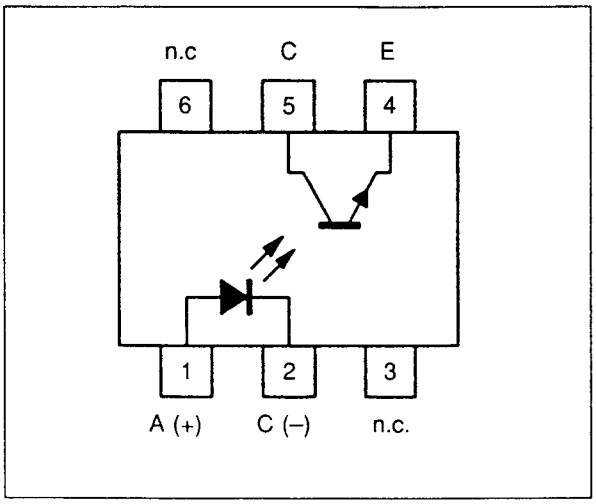
- Rated impulse voltage (transient overvoltage)
  VIOTM = 6 kV peak
- Isolation test voltage (partial discharge test voltage)
  Vpd = 1.6 kV
- Rated isolation voltage (RMS includes DC)
  VIOWM = 600 VRMS (848 V peak)
- Rated recurring peak voltage (repetitive)
  VIoRM = 600 VRMS
- Creepage current resistance according to
  VDE 0303/1EC 112
  Comparative Tracking Index: CTI = 275
- Thickness through insulation ≥ 0.75 mm
- Further approvals:
  BS 415, BS 7002, SETI: IEC 950,
  UL 1577: File No: E 76222
- Base not connected
- CTR offered in 4 groups
- Isolation materials according to UL94-VO
- Pollution degree 2 (DIN/VDE 0110 / resp. IEC 664)
- Climatic classification
  55/100/21 (IEC 68 part 1)
- Special construction:
  Therefore extra low coupling capacity of typical
  0.2 pF, high Common Mode Rejection
- Low temperature coefficient of CTR

ORDER SCHEMATIC

PART NUMBERS	CTR-RANKING
TCDT1100/TCDT1100G	>40%
TCDT1101/TCDT1101G	40 to 80%
TCDT1102/TCDT1102G	63 to 125%
TCDT1103/TCDT1103G	100 to 2000%

Suffix: G = Leadform 10.16 mm

Pin Connection



ABSOLUTE MAXIMUM RATINGS

Input (Emitter)

Parameters	Test Conditions	Symbol	Value	Unit
Reverse voltage		V_R	5	V
Forward current		I_F	60	mA
Forward surge current	$t_p \leq 10\mu s$	I_{FSM}	3	A
Power dissipation	$T_{amb} \leq 25$ °C	P_v	100	mW
Junction temperature		T_j	125	°C

Output (Detector)

Parameters	Test Conditions	Symbol	Value	Unit
Collector emitter voltage		V_{CEO}	32	V
Emitter collector voltage		V_{ECO}	7	V
Collector current		I_C	50	mA
Collector peak current	$t_p/T = 0.5$, $t_p \leq 10$ms	I_{CM}	100	mA
Power dissipation	$T_{amb} \leq 25$ °C	P_v	150	mW
Junction temperature		T_j	125	°C

Coupler

Parameters	Test Conditions	Symbol	Value	Unit
Isolation test voltage (RMS)		V_{IO}	3.75	kV
Total power dissipation	$T_{amb} \leq 25$ °C	P_{tot}	250	mW
Ambient temperature range		T_{amb}	-55 to +100	°C
Storage temperature range		T_{stg}	-55 to +125	°C
Soldering temperature	2 mm from case $t \leq 10$ s	T_{sd}	260	°C

BU2508AF
Silicon Diffused Power Transistor

GENERAL DESCRIPTION

Enhanced performance, new generation, high voltage, high-speed switching npn transistor in a plastic full-pack envelope intended for use in horizontal deflection circuits of colour television receivers. Features exceptional envelope to base drive and collector current load variations resulting in a very low worst case dissipation.

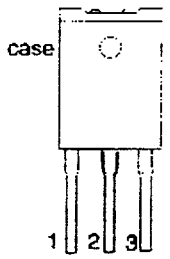
QUICK REFERENCE DATA

Symbol	Parameter	Conditions	Typ.	Max.	Unit
V_{CESM}	collector - emitter voltage peak value	V_{BE} = 0V	–	1500	V
V_{CEO}	collector - emitter voltage (open base)		–	700	V
I_C	collector current (DC)		–	8	A
I_{CM}	collector current peak value		–	15	A
P_{tot}	total power dissipation	$T_{hs} \leq 25$ °C	–	45	W
V_{CEsat}	collector - emitter saturation voltage	I_C = 4.5 A; I_B = 1.1 A	–	1	V
I_{Csat}	collector saturation current		4.5	–	A
t_f	fall time	I_{Csat} = 4.5 A; $I_{B(end)}$ = 1.1 A	0.4	0.6	µs

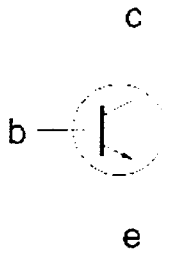
PINNING - SOT199

Pin	Description
1	base
2	collector
3	emitter
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

Symbol	Parameter	Conditions	Typ.	Max.	Unit
V_{CESM}	collector - emitter voltage peak value	V_{BE} = 0V	–	1500	V
V_{CEO}	collector - emitter voltage (open base)		–	700	V
I_C	collector current (DC)		–	8	A
I_{CM}	collector current peak value		–	15	A
I_B	Base current (DC)	$T_{hs} \leq 25$ °C	–	4	A
I_{BM}	Base current peak value	I_C = 4.5 A; I_B = 1.1 A	–	6	mA
$-I_{B(AV)}$	Reverse base current		–	100	mA
$-I_{BM}$	Reverse base current peak value[1]	I_{Csat} = 4.5 A; $I_{B(end)}$ = 1.1 A	–	5	A
P_{tot}	Total power dissipation	$T_{hs} \leq 25$ °C	–	45	W
T_{stg}	Storage temperature		-65	150	°C
T_j	Junction temperature		–	150	°C

THERMAL RESISTANCES

Symbol	Parameter	Conditions	Typ.	Max.	Unit
$R_{th\ j\text{-}hs}$	Junction to heatsink	without heatsink compound	–	3.7	K/W
$R_{th\ j\text{-}hs}$	Junction to heatsink	with heatsink compound	–	2.8	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	in free air	35	–	K/W

ISOLATION LIMITING VALUE & CHARACTERISTICS

T_{hs} = 25 °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	Repetitive peak voltage from all three terminals to external heatsink	R.H.≤ 65%; clean and dustfree	–		2500	V
C_{isol}	Capaticance from T2 to external heatsink	f= 1 MHz	–	22	–	pF

STATIC CHARACTERISTICS

T_{hs} = 25 °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{ces}	Collector cut-off current [2]	V_{BE} = 0V; V_{CE} = $V_{CESMmax}$	–	–	1.0	mA
I_{ces}		V_{BE} = 0V; V_{CE} = $V_{CESMmax}$; T_j = 125°C	–	–	2.0	mA
	Emitter cut-off current	V_{EB} = 7.5V; I_C = 0A	–	–	1.0	mA
BV_{EBO}	Emitter -base breakdown voltage	I_B =1 mA	7.5	13.5	–	V
$V_{CEOsust}$	Collector-emitter sustaining voltage	I_B = 0A; I_c = 100 mA; L = 25 mH	700	–	–	V
V_{CEsat}	Collector-emitter saturation voltages	I_C = 4.5A; I_B = 1.1A;	–	–	1.0	V
V_{BEsat}	Base-emitter saturation voltages	I_C = 4.5A; I_B = 1.7A;	–	–	1.1	V
h_{FE}	DC current gain	I_C = 100 mA; V_{CE} = 5V	–	13	–	
		I_C = 4.5A; V_{CE} = 1V	4	5.5	7.0	

DYNAMIC CHARACTERISTICS

T_{hs} = 25 °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
C_c	Collector capacitance	I_E = 0A; V_{CB} = 10V; f = 1 MHz	80	–	pF
	Switching times (16 kHz line deflection circuit)	I_{Csat} = 4.5A; $I_{B(end)}$ = 1.1A; L_B = 6 µH; $-V_{BB}$ = 4V; ($-d_B/dt$ = 0.6 A/µs)			
	Turn-off storage time		5.0	6.0	µs
t_f	Turn-off fall time		0.4	0.6	µs
	Switching times (38 kHz line deflection circuit)	I_{Csat} = 4.0A; $I_{B(end)}$ = 0.9A; L_B = 6 µH; $-V_{BB}$ = 4V; ($-dI_B/dt$ = 0.6 A/µs)			
t_s	Turn-off storage time		4.7	5.7	µs
t_f	Turn-off fall time		0.25	0.35	µs

2 Measured with half sine-wave voltage (curve tracer)

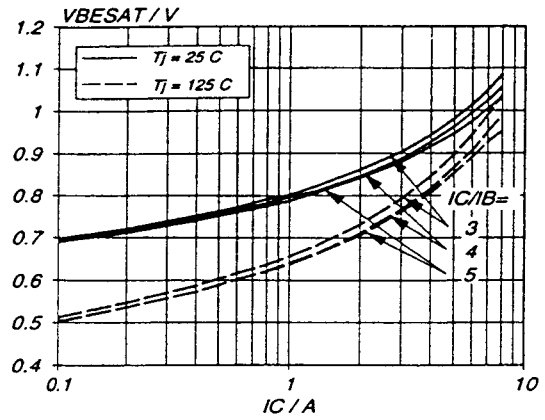


Fig. 7 Typical base-emitter saturation voltage.
$V_{BE}sat = f(I_C)$; parameter I_C/I_B

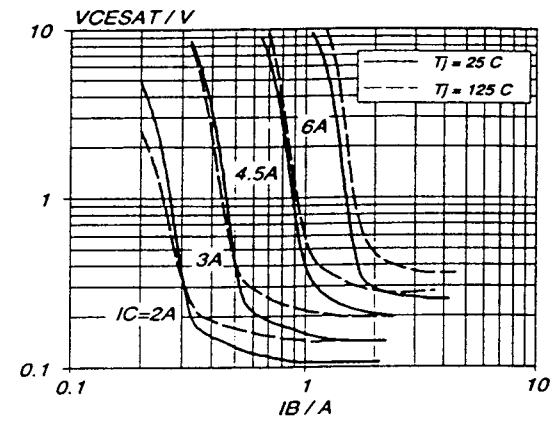


Fig. 10 Typical collector-emitter saturation voltage.
$V_{CE}sat = f(I_B)$; parameter I_C

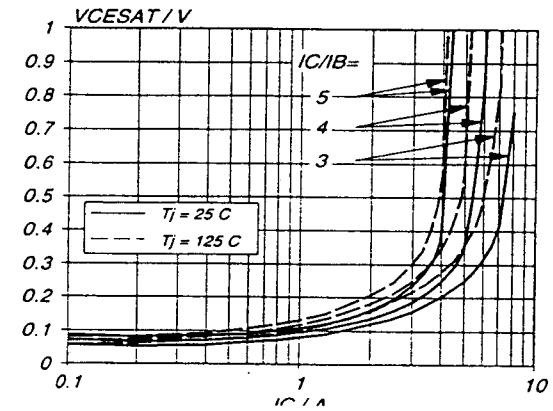


Fig. 8 Typical collector-emitter saturation voltage.
$V_{CE}sat = f(I_C)$; parameter I_C/I_B

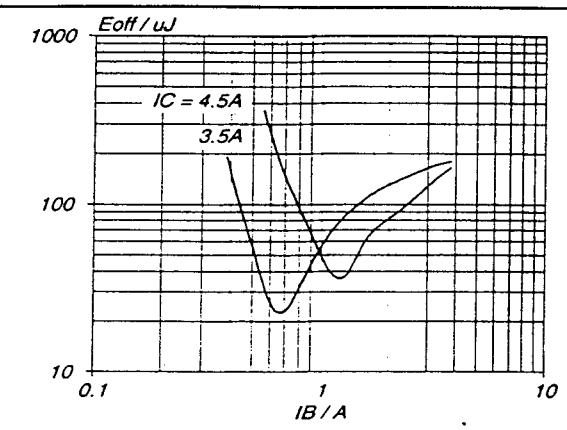


Fig. 11 Typical turn-off losses. Ti = 85 °C
$E_{off} = f(I_B)$; parameter I_C; f = 16 kHz

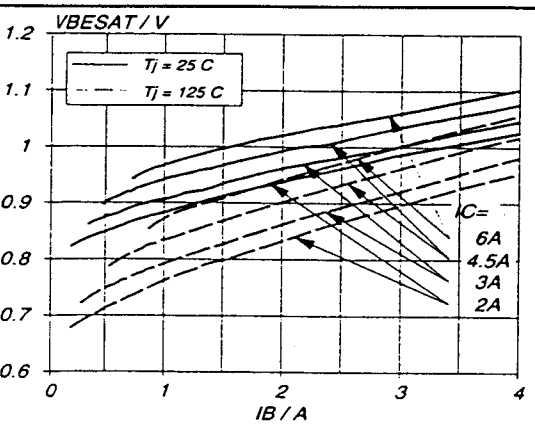


Fig. 9 Typical base-emitter saturation voltage.
$V_{BE}sat = f(I_B)$; parameter I_C

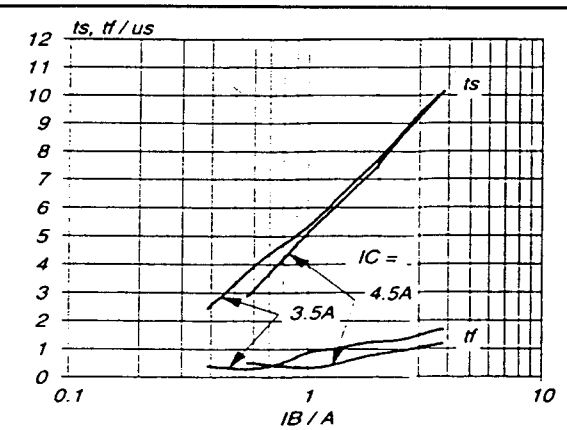


Fig. 12 Typical collector storage and fall time.
ts = f (I_B); tf = f (I_B); parameter I_C; T_j =85 °C; f = 16 kHz

BU2508DF
Silicon Diffused Power Transistor

GENERAL DESCRIPTION

High voltage, high-speed switching non transistor in a fully isolated SOT199 envelope with integrated efficiency diode, primarily for use in horizontal deflection circuits of colour television receivers.

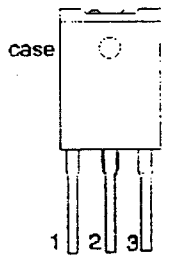
QUICK REFERENCE DATA

Symbol	Parameter	Conditions	Typ.	Max.	Unit
V_{CESM}	collector - emitter voltage peak value	V_{BE} = 0V	–	1500	V
V_{CEO}	collector - emitter voltage (open base)		–	700	V
I_C	collector current (DC)		–	8	A
I_{CM}	collector current peak value		–	15	A
P_{tot}	total power dissipation	$T_{hs} \leq 25$ °C	–	45	W
V_{CEsat}	collector - emitter saturation voltage	I_C = 4.5 A; I_B = 1.1 A	–	1	V
I_{Csat}	collector saturation current	f = 16 kHz	4.5	–	A
V_f	diode forward voltage	I_F = 4.5 A	1.6	2.0	V
t_f	fall time	I_{Csat} = 4.5 A; f = 16 kHz	0.7	–	µs

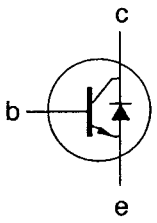
PINNING - SOT199

Pin	Description
1	base
2	collector
3	emitter
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

Symbol	Parameter	Conditions	Typ.	Max.	Unit
V_{CESM}	collector - emitter voltage peak value	V_{BE} = 0V	–	1500	V
V_{CEO}	collector - emitter voltage (open base)		–	700	V
I_C	collector current (DC)		–	8	A
I_{CM}	collector current peak value		–	15	A
I_B	Base current (DC)		–	4	A
I_{BM}	Base current peak value		–	6	A
P_{tot}	Total power dissipation	$T_{hs} \leq 25$ °C	–	34	W
T_{stg}	Storage temperature		-65	150	°C
T_j	Junction temperature		–	150	°C

THERMAL RESISTANCES

Symbol	Parameter	Conditions	Typ.	Max.	Unit
$R_{th\ j\text{-}hs}$	Junction to heatsink	without heatsink compound	–	3.7	K/W
$R_{th\ j\text{-}hs}$	Junction to heatsink	with heatsink compound	–	2.8	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	in free air	35	–	K/W

ISOLATION LIMITING VALUE & CHARACTERISTICS

T_{hs} = 25 °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	Repetitive peak voltage from all three terminals to external heatsink	R.H.≤ 65%; clean and dustfree	–		2500	V
C_{isol}	Capaticance from T2 to external heatsink	f= 1 MHz	–	22	–	pF

STATIC CHARACTERISTICS

T_{hs} = 25 °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{ces}	Collector cut-off current [2]	V_{BE} = 0V; V_{CE} = $V_{CESMmax}$	–	–	1.0	mA
I_{ces}		V_{BE} = 0V; V_{CE} = $V_{CESMmax}$; T_j = 125°C	–	–	2.0	mA
$V_{CEOsust}$	Collector-emitter sustaining voltage	I_B = 0A; I_c = 100 mA; L = 25 mH	700	–	–	V
V_{CEsat}	Collector-emitter saturation voltages	I_C = 4.5A; I_B = 1.1A;	–	–	1.0	V
V_{BEsat}	Base-emitter saturation voltages	I_C = 4.5A; I_B = 2.0A;	–	–	1.1	V
h_{FE}	DC current gain	I_C = 100 mA; V_{CE} = 5V	6	13	30	
V_F	Diode forward voltage	I_F = 4.5A	–	1.6	2.0	V

DYNAMIC CHARACTERISTICS

T_{hs} = 25 °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
f_t	Transition frequency at f = 5 MHz	I_C = 0.1 A; V_{CE} = 5V	7	–	MHz
C_c	Collector capacitance	V_{CB} = 10V	125	–	pF
	Switching times (16 kHz line deflection circuit)	I_{Csat} = 4.5A; I_C 1MHz; C_{FB} = 4 nF $I_{B(end)}$ = 1.4A; L_B = 6 µH; V_{BB} = -4 V; $-I_{BM}$ = 2.25A			
t_s	Turn-off storage time		6.5	–	µs
t_f	Turn-off fall time		0.7	–	µs

1 Measured with half sine-wave voltage (curve tracer)

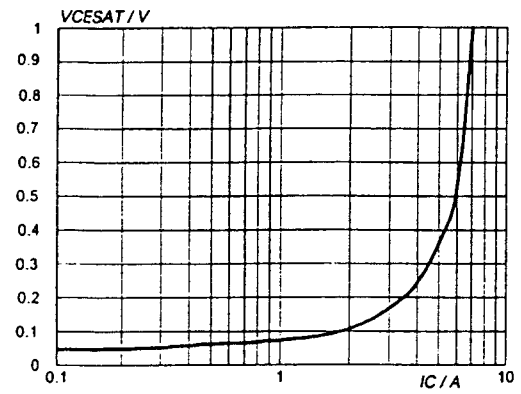


Fig. 5 Typical collector-emitter saturation voltage.
$V_{CE}sat = f(I_C)$; parameter I_C/I_B

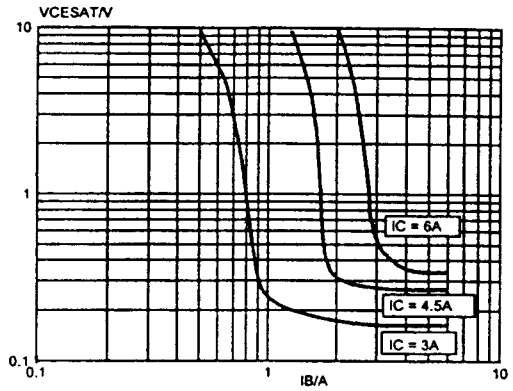


Fig. 7 Typical collector-emitter saturation voltage.
$V_{CE}sat = f(I_B)$; parameter I_C

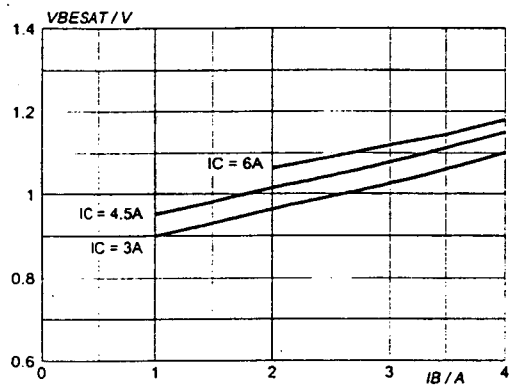


Fig. 6 Typical base-emitter saturation voltage.
$V_{BE}sat = f(I_C)$; parameter I_C

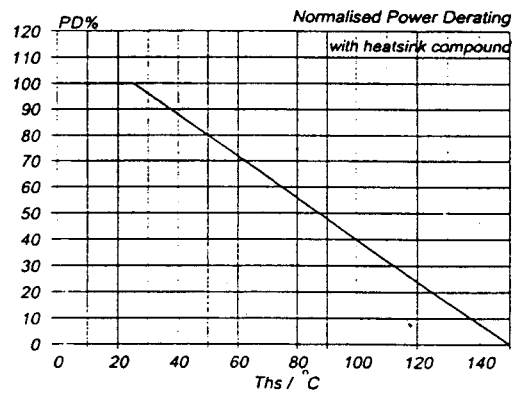
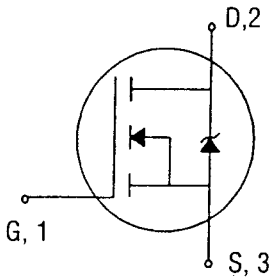
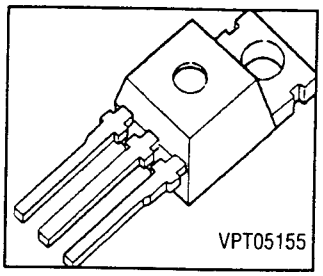


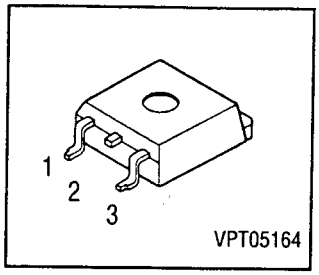
Fig. 8 Normalised power dissipation
$PD\% = 100\ P_D/P_{D\ 25°C} = f(T_{hs})$;

SPP03N60S5 / SPB03N60S5
Cool MOS Power Transistor

- New revolutionary high voltage technology
- Ultra low gate charge
- Periodic avalanche proved
- Extreme dv/dt rated
- Optimized capacitances
- Improved noise immunity
- Former development designation: SPPx4N60S5/SPBx4N60S5







Type	V_{DS}	I_D	$R_{DS(on)}$	Package	Marking	Ordering Code
SPP03N60S5	600V	3.2A	1.4Ω	P-TO220-3-1	03N60S5	Q67040-S4184
SPB03N60S5				P-TO263-3-2	03N60S5	Q67040-S4197

MAXIMUM RATINGS

at T_j = 25 °C; unless otherwise specified

Parameter	Symbol	Value	Unit
Continuous drain current T_C = 25 °C T_C = 100 °C	I_D	 3.2 2	A
Pulsed drain current, tp = 1ms (1) T_C = 25 °C	$I_{D\ puls}$	5.7	
Avalanche energy, single pulse I_D =3.2A, V_{DD} = 50V, R_{GS} = 25Ω Periodic avalanche energy E_{AR} only limited by T_{jmax}	E_{AS}	100	mJ
Reverse diode d_v/d_t IS = 3.2 A, V_{DS}<V_{DSS}, d_i/d_t = 100 A/µs, T_{jmax} = 150 °C	d_v/d_t	6	kV/µs
Gate source voltage	V_{GS}	±20	V
Power dissipation T_C = 25 °C	P_{tot}	38	°C
Operating and storage temperature	T_j, T_{stg}	-55 ...+150	°C

ELECTRICAL CHARACTERISTICS

Parameter at T_j = 25 °C; unless otherwise specified	Symbol	Value			Unit
		min.	typ.	max.	

Thermal Characteristics

Thermal resistance, junction - case	R_{thJC}	–	–	3.3	K/W
Thermal resistance, junction - ambient (Leaded and through-hole packages)	R_{thJA}	–	–	62	
SMD version, device on PCB @ min. footprint @ 6 cm² cooling area [2]	RthJA	 –	 –	 62	
		–	35	–	

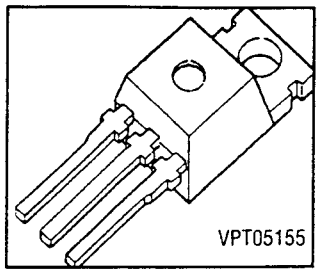
Static Characteristics

Drain-source breakdown voltage V_{GS} = 0V, I_D = 0.25 mA	$V_{(BR)DSS}$	600	–	–	V
Gate threshold voltage, V_{GS} = V_{DS} I_D = 135 µA, T_j = 25 °C	$V_{GS(th)}$	3.5	4.5	5.5	
Zero gate voltage drain current, V_{DS} = V_{DSS} V_{GS} = 0V, T_j = 25 °C V_{GS} = 0V, T_j = 150 °C	I_{DSS}	 –	 0.5	 1	µA
		–	–	70	
Gate-source leakage current V_{GS} = 20V, V_{DS} = 0V	I_{GSS}	–	–	100	nA
Drain Source on-state resistance V_{GS} = 10V, I_D = 2A	$R_{DS(on)}$	–	1.26	1.4	Ω

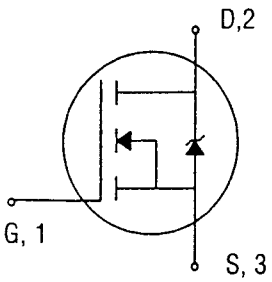
[1] current limited by T_{jmax}

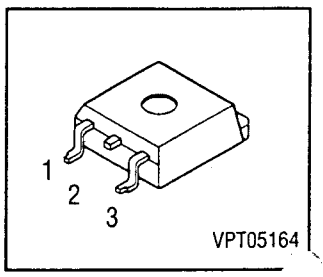
[2] Device on 50mm*50mm*1.5mm epoxy PCB FR4 with 6 cm2 (one layer, 70µm thick) copper area for drain connection. PCB is vertical without blown air.

SPP04N60S5 / SPB04N60S5
Cool MOS Power Transistor



- New revolutionary high voltage technology
- Ultra low gate charge
- Periodic avalanche proved
- Extreme d_V/d_t rated
- Optimized capacitances
- Improved noise immunity
- Former development designation: SPPx6N60S5/SPBx6N60S5





Type	V_{DS}	I_D	$R_{DS(on)}$	Package	Marking	Ordering Code
SPP04N60S5	600V	4.5A	0.95Ω	P-TO220-3-1	04N60S5	Q67040-S4200
SPB04N60S5				P-TO263-3-2	04N60S5	Q67040-S4201

MAXIMUM RATINGS

at T_j = 25 °C; unless otherwise specified

Parameter	Symbol	Value	Unit
Continuous drain current T_C = 25 °C T_C = 100 °C	I_D	 4.5 2.8	A
Pulsed drain current, tp = 1ms (1) T_C = 25 °C	$I_{D\ puls}$	7.7	
Avalanche energy, single pulse I_D = 4.5A, V_{DD} = 50V, R_{GS} = 25Ω Periodic avalanche energy E_{AR} only limited by T_{jmax}	E_{AS}	130	mJ
Reverse diode d_V/d_t I_S = 4.5 A, V_{DS}<V_{DSS}, d_i/d_t = 100 A/µs, T_{jmax} = 150 °C	d_V/d_t	6	kV/µs
Gate source voltage	V_{GS}	±20	V
Power dissipation T_C = 25 °C	P_{tot}	50	W
Operating and storage temperature	T_j, T_{stg}	-55 ...+150	°C

ELECTRICAL CHARACTERISTICS

Parameter at T_j = 25 °C; unless otherwise specified	Symbol	Value			Unit
		min.	typ.	max.	

Thermal Characteristics

Thermal resistance, junction - case	R_{thJC}	–	–	2.5	K/W
Thermal resistance, junction - ambient (Leaded and through-hole packages)	R_{thJA}	–	–	62	
SMD version, device on PCB @ min. footprint @ 6 cm^2 cooling area [2]	RthJA	 – –	 – 35	 62 –	

Static Characteristics

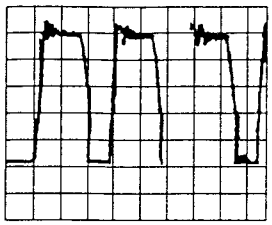
Drain-source breakdown voltage V_{GS} = 0V, I_D = 0.25 mA	$V_{(BR)DSS}$	600	–	–	V
Gate threshold voltage, V_{GS} = V_{DS} I_D = 200 µA, T_j = 25 °C	$V_{GS(th)}$	3.5	4.5	5.5	
Zero gate voltage drain current, V_{DS} = V_{DSS} V_{GS} = 0V, T_j = 25 °C V_{GS} = 0V, T_j = 150 °C	I_{DSS}	 – –	 0.5 –	 1 50	µA
Gate-source leakage current V_{GS} = 20V, V_{DS} = 0V	I_{GSS}	–	–	100	nA
Drain Source on-state resistance V_{GS} = 10V, I_D = 2.8A	$R_{DS(on)}$	–	0.85	0.95	Ω

[1] current limited by T_{jmax}

[2] Device on 50mm*50mm*1.5mm epoxy PCB FR4 with 6 cm2 (one layer, 70µm thick) copper area for drain connection. PCB is vertical without blown air.

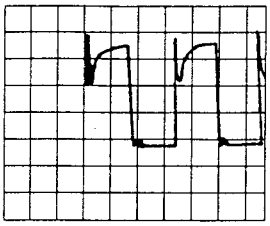
OSCILLOSCOPE SHAPES

1) 5usn/div 100 volt/div



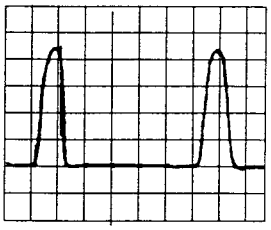
Drain of TP01

2) 20msn/50 volts/div



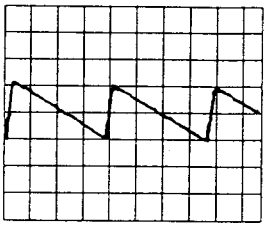
Collector of TD01

3) 10 usn/div 250 volt/div



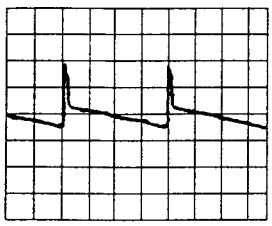
Collector of TD02

4) 5 msn/div 0.5 volt/div



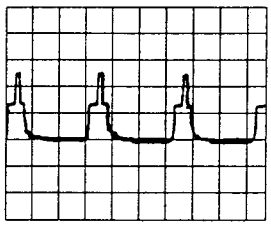
I V01 pin 22

5) 5msn/div 20 volts/div



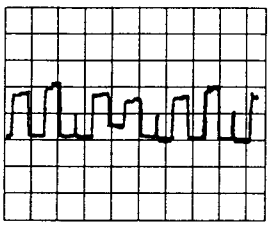
I D50 pin 4

6) 20usn/2 volts/div



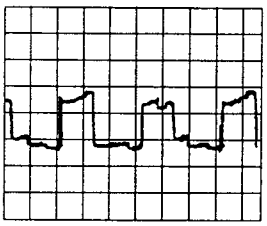
I V01 pin 34

7) 20usn/2 volts/div



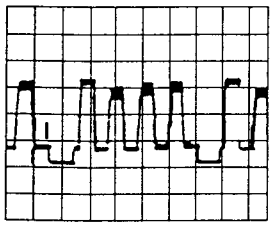
I V01 pin 48

8) 20usn/2 volts/div



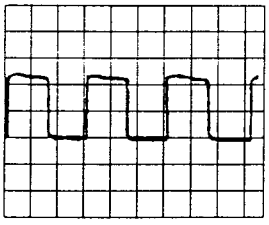
I V01 pin 47

9)10 usn/2 volts/div



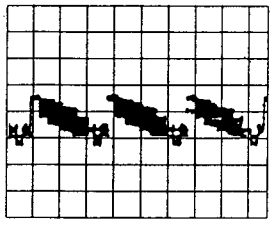
I V01 pin 46

10) 20 usn/0.5 volt/div

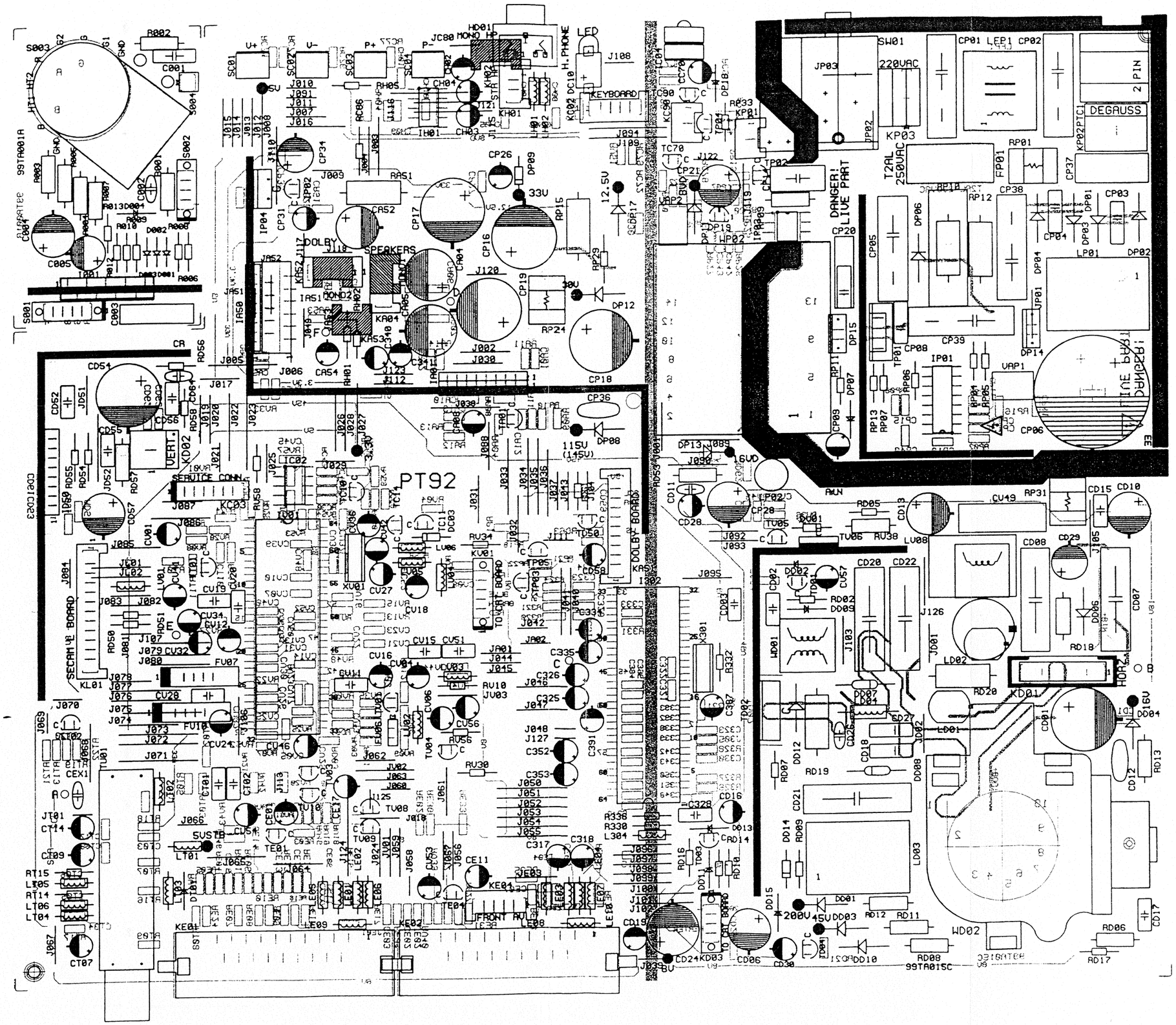


I V01 pin 33

11) 20usn/1 volt/div



I V01 pin 40


PT92
SECAM/E BOARD
SERVICE CONN.
SUSTB
VERT.
DOLBY BOARD
TOWER BOARD
FRONT AV
KEYBOARD
H.PHONE
MONO HP
DEGAUSS
220VAC
T2AL 250VAC
DANGER! LIVE PART
SPEAKERS
DOLBY
33V
30V
16VD
115V (145V)
200V
WD02
99TA01SC

SOUND PROCESSOR

I302 — TDA9875A

PCLK, NICAM, ADDR1, SCL, SDA, VSSA1, VDDA1, I-REF, P1, SIF2, V-REF1, SIF1, ADDR2, V-SSD1, V-DDD1, CRESET, XTAL0, XTAL1, V-TUNE, P2, SYSCLK, SCK, WS, SDO2, SDO1, SDI2, SDI1, TEST1, MONO_IN, TEST2, EXTIR, EXTIL

V-DDD2, LOR, LOL, MOL, MOR, V-DDA3, AUXOL, AUXOR, V-SSA3, PCAPL, PCAPR, V-REF3, SCOL2, SCOR2, V-SSA4, V-SSD2, SCOL1, SCOR1, V-REF2, CAPR1, CAPR2, VSSA2, CAPL2, CAPL1, V-REF(N), W-REF(P), VDDA2, SCIL2, SCIR2, VSSG, SCIL1, SCIR1

R330 1R 5V; C349 470NF 50V

R326 100R SCL; R327 100R SDA

C330 470NF; R328 10K

DOLBY J305; C329 100NF; QSSO; L304 1uH; C327 47PF 50V

R332 1R 5V; C331 470NF; C387 1MF 50V; C321 10PF 50V; X301 24.576MHz; C322 10PF 50V

SCK; WS; SDO1; SDI2; SDI1; AMOUT; C328 470NF

C351 0NF 50V; C350 0NF 50V

C353 2M2F 50V TV-S/L; C352 2M2F 50V TV-S/R

R336 1R 5V; C341 2M2F 50V HPL; C340 2M2F 50V HPR

C348 470NF; C343 10NF; C342 150NF 50V; C339 10NF 50V; C338 10NF 50V; C391 47MF 25V

C317 10MF 50V SC2OUTL; C318 10MF 50V SC2OUTR

C392 470PF; C393 470PF; C394 470PF; C395 470PF

C325 10MF 50V SC1OUTL; C326 10MF 50V SC1OUTR

C335 47MF 25V

C334 47MF 25V; R331 270R; C333 470NF

C320 330NF; R321 15K SC2IL; C319 330NF; R320 15K SC2IR

C324 330NF; R325 15K E.AUD; C323 330NF; R324 15K SC1IR

TUNER

TU01 — UV1315 (UV1316 FOR PLL)

SCL; SDA; AGC; IF1; IF2; SVSTB; BND0; BND1

33V; CT03 100NF 50V; RT02 12K; RT03 15K; RT05 47K; CT01 100NF 50V; CT02 100NF 63V; RT01 220R; CT10 8P2 50V; TT01 PH2369; V.TUNE; RT12 1K; RT11 180R

RT14 100R; RT15 100R *; LT03; LT04 1uH; LT05 3u3H; LT06 3u3H

RT07 3K9; RT08 15K; FOR SECAM; D101 1N4148; RT09 12K; ELSE (D101 JUMPER)

CT08 100NF 50V; CT09 10NF 50V; LT01 1u7H; LT02 1uH; CT11 68P 500V; ASYM.TUNER; JT01

CT14 10NF 50V; RT18 22K; 33V; CEX1 XXXX 100V

RT16 1K; RT17 0R; CT04 100NF 50V; CT05 100NF 50V; CT06 100NF 50V; CT07 47NF 25V; CT17 100NF 50V

8V; RT19 3K3; RT20 3K3; RT21 3K3

TT02 BC547B; RT22 47K; RT13 47K

* : FOR PLL TUNER

AUDIO AMPLIFIER

IA01 — TDA2615 (TDA2616)

-INV1, MUTE, 1/2VP/GND, OUT1, -VP, OUT2, +VP, INV1,2, -INV2

TV-S/R; RA09 3K9; RA10 750R (1K); CA01 470NF 50V; RA11 3K9; CA12 2N2F 50V; CA13 2N2F 50V; RA14 3K9; CA02 470NF 50V; RA12 3K9; RA13 750R (1K)

VIN; TV-S/L; MONO AUDOUT; JA01; TV-S/R; JA02 28"MONO

30V; CA06 22NF 50V; CA07 22NF 50V; RA08 22K; RA06 8R2; RA07 8R2; CA10 100NF 50V; CA05 1000MF 25V; CA04 1000MF 25V; KA04 SPEAKERS; STEREO

MUTEM; MUTE; RA05 1K; RA04 4K7; CA11 68NF 50V; TA01 BC547B; CA08 100MF 63V

RESET

RC59 10K; RC58 10K; RC52 100R; RC25 47K; +VMICRO; TC11 BC556B; TC14 BC556B; DC03 2V4; RC60 10K; +VMEM; RESET; RC26 22K; TC10 BC547B

EEPROM

IC02 — 24C16

A0, A1, A2, VSS, VDD, PTC, SCL, SDA

+VMEM; CV45 100NF 50V; JC01; RC46 3K3; RC42 3K3; RC47 100R; RC30 100R; SCL1; SDA1

uCONTROLLER+VIDEO PROCESSOR

IV01 — TDA9351X/6X/8X

+VMICRO; 5V; AV32 1K2; AV33 1K2; CV01 10NF 50V; AV01 3K3; AV02 3K3; AV08 3K3; AV05 100R

SCL; SDA; V.TUNE; MUTE; AV1/AV2; KEYB; STAT-AV; SW0; SW1; AMOUT; EX.AUD; B/G-SND

AV24 100R; AV28 100R; AV58 100R; AV29 47R; AV04 100R

P1.3/T1, P1.6/SCL, P1.7/SDA, P2.0/TPWM, P3.0/ADC0, P3.1/ADC1, P3.2/ADC2, P3.3/ADC3, VSSC/P, P0.5, P0.6, VSSA, SECPLL, VP2, DECDIG, PH2LF, PH1LF, GND3, DECBG, AVL/EWD, VDRB, VDRA, IFIN1, IFIN2, IREF, VSC, AGCOUT, AUDEEM/SIFIN1, DECSDEM/SIFIN2, GND2 AUDEXT/QSSO/AMOUT, SNDPLL/SIFAGC, AVL/REFO/AMOUT

P1.2/INT0, P1.1/T0, P1.0/INT1, VDDP, RESET, XTALOUT, XTALIN, OSCGND, VDDC, VPE, VDDA, BO, GO, RO, BLKIN, BCLIN, B2/VIN, G2/YIN, R2/VIN, INSSW2, AUDOUT/AMOUT, CHROMA, CVBS/Y, GND1, CVBSINT, VP1, IFVO, PLLIF, EHTO, FBISO, HOUT

8V; LV01 10uH; CV40 100NF 50V; CV41 100NF 16V; CV19 220NF 63V; CV20 220NF 63V; CV35 2N2F 50V; AV27; CV34 1NF 50V; AV22 15K; CV33 4N7F 50V; CV13 100NF 50V; CV12 2N2F 50V; CV32 4N7F 50V; CV31 1N2F 50V; CV30 1N2F 50V

E/WDRIVE; IDRIVE-; IDRIVE+; RD50 100R; RD51 100R; 4

IF1; IF2; FV07 K2966M; AV22 39K; CV28 100NF 63V

AGC; IF1_S; IF2_S; AV21 680R; FV10 K9453M; CV26 10NF 50V; CV25 4N7F 50V; CV24 33NF 16V; CV02 820PF 50V; CV05 4N7F 50V; AV52 2K7; AV07 100R

8V; AV18 820R; AV19 1K5; TV03 BC547B; AV20 330R

+VMICRO; AV30 470R

HEADPHONE AMPLIFIER

HD01; JC00 STEREO; LH02 22uH; LH01 22uH; KH01 STA-HP; KH02 MONO-HP; SPK 100R; OUT2-RC86; OUT2+

CH06 47NF 50V; CH03 100NF 16V; CH05 47NF 50V; CH04 100NF 16V; CH08 2N2F 50V; CH07 2N2F 50V

IH01 — TDA7050

GND, OUTA, OUTB, VDD, INB-POS, INB-NEG, INA-NEG, INA-POS

RH01 10K HPR; RH02 10K HPL; RH04 680R; RH03 680R; CH09 2N2F 50V; CH10 2N2F 50V

RH05 4R7 5V; CH02 100MF 16V; CH01 100NF 50V

E.AUD; SC1IR; SC1OUTL; SC1OUTR; B/G-SND; SC2IL; SC2IR

RE25 12K; RE26 12K; CE07 1NF 50V; CE08 1NF 50V; RE28 12K; RE29 12K; LE07 8u2H; LE08 8u2H

CE17 10NF 50V; LE01 8u2H; LE02 8u2H; CE05 1NF 50V; CE04 1NF 50V; 8V; RE30 10R; CE11 10NF 50V; TE04 BC547B; RE33 100R

CE03 1NF 50V; CE02 1NF 50V; JE02 MONO; RE17 12K; RE34 12K; LE06 8u2H; RE14 12K; RE15 12K; LE05 8u2H

BIN; STAT-AV; GIN; RIN; FBLIN

CE12 120PF 50V; CE16 120PF 50V; RE11 4K7; CE13 120PF 50V; CE14 120PF 50V; CE15 120PF 50V

E.AUD; JE03 MONO; JE04; SC2IR; SC2IL; FRONTAU; CVBSEXT2; KE04; RE03 10R; 8V; CE01 10NF 50V; RE02 100R; TE01 BC547B; TU.VID

TU01

UV1315 (UV1316 FOR PLL)

AGC, TUN, VHF, VHF3, VHF1, 5V, AFT, NC, NC, IF2, IF1

FOR SECAM

IF1

IF2

5VSTB

ASYN.TUNER

33V

BND0

BND1

* : FOR PLL TUNER

AUDIO AMPLIFIER

DA2615 (TDA2616)

OUT1, -VP, OUT2, +VP, INV1,2, -INV2

VIN

TV-S/L

TV-S/R

MONO AUDOUT

28"MONO

SPEAKERS

STEREO

EEPROM

IC02

24C16

+VMEM

SCL1

SDA1

uCONTROLLER+VIDEO PROCESSOR

IV01

TDA9351/6X/8X

+VMICRO, 5V, +VMEM, 8V

SCL, SDA, V.TUNE, MUTE, AV1/AV2, KEYB, STAT-AV, SW0, SW1, E/WDRIVE, IDRIVE-, IDRIVE+, IF1, IF2, AGC, IF1_S, IF2_S, AMOUT, EX.AUD, B/G-SND

P1.3/T1, P1.6/SCL, P1.7/SDA, P2.0/TPWM, P3.0/ADC0, P3.1/ADC1, P3.2/ADC2, P3.3/ADC3, VSSC/P, P0.5, P0.6, VSSA, SECPLL, VP2, DECDIG, PH2LF, PH1LF, GND3, DECBG, AVL/EWD, VDRB, VDRA, IFIN1, IFIN2, IREF, VSC, AGCOUT, AUDEEM/SIFIN1, DECSDEM/SIFIN2, GND2 AUDEXT/QSSO/AMOUT, SNDPLL/SIFAGC, AVL/REFO/AMOUT

P1.2/INT0, P1.1/T0, P1.0/INT1, VDDP, RESET, XTALOUT, XTALIN, OSCGND, VDDC, VPE, VDDA, BO, GO, RO, BLKIN, BCLIN, B2/VIN, G2/YIN, R2/VIN, INSSW2, AUDOUT/AMOUT, CHROMA, CVBS/Y, GND1, CVBSINT, VP1, IFVO, PLLIF, EHTO, FBISO, HOUT

LED, ST-BY, RMOT, SDA1, SCL1, +VMICRO, RESET, BCL, BIN, GIN, RIN, FBLIN, AUDOUT, AV.VID, QSSO, CVBSINT, BCUR, QSSO, E.AUD, H_FLYBACK, H_DRIVE

TO-CRT-BOARD KV01

FV07 K2956M

FV10 K9453M

FV06 TPWA02B

TV01 BC556B, TV02 BC547B, TV03 BC547B, TV04 BC547B, TV08 BC547B, TV09 BC547B, TV10 BC547B, TE01 BC547B, TE04 BC547B, TC70 BC547B, TC10 BC547B

DOLBY AMPLIFIER

IA51 TDA7057AQ

U.CN1, N.C., VIN1, VSUP, VIN2, SGND, U.CN2, OUT2+, PGND2, OUT2-, OUT1-, PGND1, OUT1+

HPR, HPL, MUTEM, VSUP, 12.5V

JUMPER

OUT2-, OUT2+

KA52 DOLBY

MONO/OPT.

IA50 TDA7056A

N.C., VSUP, VIN, GND1, VCNT, OUT+, GND2, OUT-, N.C.

VSUP, VIN, MUTEM

OUT2+, OUT2-, SPK

KA52 SINGLE-SPK

KA53 DOUBLE-SPK

SERVICE

SERVICE

KC03

SCL1, SDA1, KEYB, SCL, SDA, 5V

SECAM L MONO SOCKET

KL01

SECAM-L-MONO

SW0, BND0, BND1, SW1, 8V, EX.AUD, IF1_S, IF2_S, IF2

INFRARED MODULE

IC04

GND, IR, VCC

LOGO

TC90 BC556B

KC90, KC02

RMOT, LED, KEYB

SC02 VOL-

SC03 P+

SC04 P-

DOLBY SOCKET

DOLBY

5V, SCL, SDA, RESETMSP, SCK, WS, SDO1, SDI2, SDI1

KA51

VIDEO SWITCH

CVBSEXT2, CVBSEXT1, AV1/AV2

AV.VID

VERTICAL

ID50 TDA8356 (TDA8351)

DRV-POS, DRV-NEG, VP, VO(B), GND, VFB, VO(A), VO(GUARD), VI(FB)

IDRIVE+

BCL

HEADPHONE AMPLIFIER

CRT BOARD

RESET

EEPROM

SCARTS

POWER SUPLLY

115V +B
(145V +B)

WP02 SMT

with PFC

*VAL: 3.3uF FOR 14"
6.8uF FOR 21"
10uF FOR 28"

⚠ INDICATES SPECIALLY SELECTED OR CRITICAL SAFETY COMPONENTS AND IDENTICAL COMPONENTS SHOULD BE USED FOR THERE REPLACEMENT. THIS IS NECESSARY IN ORDER TO MAINTAIN THE OPERATIONAL SAFETY OF THE RECEIVER.

THE SERVICE INFORMATION FOR SAFETY
WHEN SERVICING THIS AREA CONNECT AN ISOLATING TRANSFORMER BETWEEN TV RECEIVER AND AC LINE TO ELIMINATE HAZARD OF ELECTRIC SHOCK.

SPEAKERS
STEREO
EEPROM
IC02
24C16
IV01
FV07 K2966M
FV10 K9453M
IFIN1
IFIN2
IREF
VSC
AGCOUT
AUDEEM/SIFIN1
DECSDEM/SIFIN2
GND2 AUDEXT/QSSO/AMOUT
SNDPLL/SIFAGC
AVL/REFO/AMOUT
CUBS/Y
GND1
CUBSINT
VP1
IFVO
PLLIF
EHTO
FBISO
HOUT
TV.VID
CUBSINT
BCUR
QSSO
E.AUD
H_FLYBACK
H_DRIVE
SERVICE
INFRARED MODULE
SECAM L MONO SOCKET
SECAM-L-MONO
DOLBY SOCKET
DOLBY
KA51
VIDEO SWITCH
E/W DRIVE
E/WDRIVE
TO-CAT-BOARD
ID50
TDA8356
(TDA8351)
VERTICAL
IDRIVE+
IDRIVE-
BCL
KD02
VERT.DEFL.YOKE
E.AUD
BIN
STAT-AV
GIN
RIN
FBLIN
FRONTAV
SC21R
SC21L
CUBSEXT2
KE04
TV.VID
SCART20´21
KE01
CUBSEXT1
115V +B POWER SUPLLY
(145V +B)
WP02 SMT
with PFC
IP01
TDA16846
IP02
LE33AB/C
IP04
LM7805
IP03
TCDT1101G
+BIN
33V
16VD
3V3
+VMICRO
5V
8VD
SVSTB
12.5V
30V
115V
ST-BY
HE SERVICE INFORMATION FOR SAFETY
WHEN SERVICING THIS AREA CONNECT
AN ISOLATING TRANSFORMER BETWEEN
TV RECEIVER AND AC LINE TO ELIMINATE
HAZARD OF ELECTRIC SHOCK.
HORIZONTAL
WD02
FBT
KD01
HOR.DEFL.YOKE
HOR.DRV.
HOR.
+BOUT
200V
HEATER
+: FOR 90DEGREE
*: FOR 110DEGREE
PT92 CHASSIS SCHEMATIC DIAGRAM
VER.C